

MIL-M-38510/28B(USAF)
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SUPERSEDING
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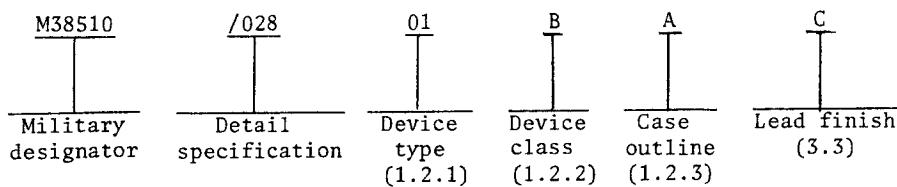
MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL TTL, LOW POWER
SHIFT REGISTERS MONOLITHIC SILICON

1. SCOPE

1.1 Scope. This specification covers the requirements for monolithic silicon, TTL, low power shift register microcircuits. Three product assurance classes and a choice of case outline/lead finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall be as shown in the following:

<u>Device type</u>	<u>Circuit</u>
01	4-bit right-shift, left-shift register
02	8-bit parallel-out, serial shift register
03	Dual, 8-bit shift register
04	4-bit shift register
05	8-bit parallel-out, serial shift register

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Letter</u>	<u>Case outline, MIL-M-38510, appendix C</u>
A	F-1 (14-pin, 1/4" x 1/4" flat pack)
B	F-3 (14-pin, 1/8" x 1/4" flat pack)
C	D-1 (14-pin, 1/4" x 3/4" dual-in-line pack)
D	F-2 (14-pin, 1/4" x 7/8" flat pack)
E	F-5 (16-pin, 1/4" x 3/8" flat pack)
F	D-2 (16-pin, 1/4" x 7/8" dual-in-line pack)

1.3 Absolute maximum ratings.

Supply voltage range	
Device type 01 - - - - -	0 Vdc to 8.0 Vdc
Device type 02 - - - - -	0 Vdc to 7.0 Vdc
Device type 03 - - - - -	-0.5 Vdc to 7.0 Vdc
Device type 04 - - - - -	-0.5 Vdc to 7.0 Vdc
Device type 05 - - - - -	0 Vdc to 7.0 Vdc
Input voltage range - - - - -	0 Vdc to 6.0 Vdc
Storage temperature range - - -	-65°C to 150°C

Maximum power dissipation per register, P_D	
Device type 01 - - - - -	20 mW
Device type 02 - - - - -	120 mW
Device type 03 - - - - -	134 mW
Device type 04 - - - - -	124 mW
Device type 05 - - - - -	52 mW
Lead temperature (soldering 10 seconds) - - - - -	300°C
Thermal resistance, junction to case - - - - -	$\theta_{JC} = \begin{cases} 0.09^\circ\text{C}/\text{mW} & \text{for flat pack} \\ 0.08^\circ\text{C}/\text{mW} & \text{for dual-in-line pack} \end{cases}$
Junction temperature - - - - -	$T_J = 175^\circ\text{C}$

1.4 Recommended operating conditions.

Supply voltage - - - - -	4.5 Vdc min to 5.5 Vdc maximum
Minimum high level input voltage - - - - -	2.0 Vdc
Maximum low level input voltage	
Device type 01 - - - - -	0.7 Vdc
Device type 02 - - - - -	0.8 Vdc
Device type 03 - - - - -	0.7 Vdc
Device type 04 - - - - -	0.7 Vdc
Device type 05 - - - - -	0.7 Vdc
Ambient operating temperature range - - - - -	-55°C to 125°C
Fanout	
Device type 01	
High logic level - - - - -	0.1 mA
Low logic level - - - - -	2.0 mA
Device type 02	
High logic level - - - - -	0.2 mA
Low logic level - - - - -	4.0 mA
Device types 03 and 04	
High logic level - - - - -	0.32 mA
Low logic level - - - - -	3.2 mA
Device type 05	
High logic level - - - - -	0.2 mA
Low logic level - - - - -	2.0 mA

2. APPLICABLE DOCUMENT

2.1 The following document, of the issue in effect on date of invitation for bids or request for proposal, forms a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 3.

3.2.4 Schematic circuit. The schematic circuit shall be as specified on figure 4.

3.2.5 Case outlines. Case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended ambient operating temperature range, unless otherwise specified.

3.5 Rebonding. Rebonding shall be in accordance with MIL-M-38510.

3.6 Electrical test requirements. Electrical test requirements shall be as specified in table III for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualification and quality conformance, by device class are specified in table II. Subgroups 7 and 8 do not apply to device type 03.

3.7 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container:

(a) Country of origin.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, and C inspections (see 4.4.1, 4.4.2, and 4.4.3). After qualification of one or more electrically and structurally similar types with a single lead finish, other lead finishes of the same case outline may be qualified by submitting a single type in the qualified case outline to the group B, subgroup 3 test and the group C, subgroups 1, 3, and 4 tests.

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

(a) Test samples for the group B bond strength test specified in method 5005 of MIL-STD-883 may, at the manufacturer's option, be randomly selected immediately following the internal visual (precap) inspection and prior to sealing (see 4.4.2(a)).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Device type	Limits		Units
				Min	Max	
High-level output voltage	V_{OH}	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2.0 \text{ V}$, $I_{OH} = -100 \mu\text{A}$, $V_{IL} = 0.7 \text{ V}$	01	2.4	---	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -200 \mu\text{A}$	02	2.4	---	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.7 \text{ V}$, $I_{OH} = -320 \mu\text{A}$	03	2.4	---	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.7 \text{ V}$, $I_{OH} = -320 \mu\text{A}$	04	2.4	---	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.7 \text{ V}$, $I_{OH} = -200 \mu\text{A}$	05	2.4	---	Volts
Low-level output voltage	V_{OL}	$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.7 \text{ V}$, $I_{OL} = 2 \text{ mA}$	01	---	0.3	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 4 \text{ mA}$	02	---	0.4	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.7 \text{ V}$, $I_{OL} = 3.2 \text{ mA}$	03	---	0.3	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.7 \text{ V}$, $I_{OL} = 3.2 \text{ mA}$	04	---	0.3	Volts
		$V_{CC} = 4.5 \text{ V}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.7 \text{ V}$, $I_{OL} = 2 \text{ mA}$	05	---	0.3	Volts
High-level input voltage	V_{IH}	$V_{CC} = 4.5 \text{ V}$	A11	2.0	---	Volts
Low-level input voltage	V_{IL}	$V_{CC} = 4.5 \text{ V}$	01,03, 04,05		0.7	Volts
		$V_{CC} = 4.5 \text{ V}$	02		0.8	Volts
High-level input current at any input except mode control	I_{IH1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	01	---	10	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$	01	---	100	μA
High-level input current at mode control	I_{IH3}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	01	---	20	μA
	I_{IH4}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$	01	---	200	μA
High-level input current	I_{IH1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	02	---	20	μA
	I_{IH2}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$	02		100	μA
High-level input current at MR, D_0 , and D_1	I_{IH1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	03		20	μA
High-level input current at CP	I_{IH2}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	03		30	μA
High-level input current at D_S	I_{IH3}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	03		40	μA
High-level input current at CP COMMON	I_{IH4}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	03		60	μA
High-level input current, all inputs	I_{IH5}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$	03		100	μA
High-level input current at J , K , MR, P_0 , P_1 , P_2 , P_3	I_{IH1}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.4 \text{ V}$	04		20	μA

TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions	Device type	Limits		Units
				Min	Max	
High-level input current at CP	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 2.4 V	04		40	μA
High-level input current at PE	I _{IH3}	V _{CC} = 5.5 V, V _{IN} = 2.4 V	04		46	μA
High-level input current, all inputs	I _{IH4}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	04		100	μA
High-level input current, except clear	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.4 V	05		10	μA
High-level input current, clear input	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 2.4 V	05		20	μA
High-level input current, except clear	I _{IH3}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	05		100	μA
High-level input current, clear input	I _{IH4}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	05		200	μA
Low-level input current at any input except mode control	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	01	-0.06	-0.18	mA
Low-level input current at mode control	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	01	-0.12	-0.36	mA
Low-level input current	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.4 V	02	-0.35	-0.8	mA
Low-level input current at MR, D ₀ and D ₁	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	03	-0.12	-0.4	mA
Low-level input current at CP	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	03	-0.25	-0.6	mA
Low-level input current at D _S	I _{IL3}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	03	-0.24	-0.8	mA
Low-level input current at CP COMMON	I _{IL4}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	03	-0.36	-1.2	mA
Low-level input current at J, K, MR, P ₀ , P ₁ , P ₂ , P ₃	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	04	-0.12	-0.4	mA
Low-level input current at CP	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	04	-0.35	-0.8	mA
Low-level input current at PE	I _{IL3}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	04	-0.36	-0.92	mA
Low-level input current, except clear	I _{IL1}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	05	-0.06	-0.18	mA
Low-level input current, clear input	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.3 V	05	-0.12	-0.36	mA
Short-circuit output current	I _{OS}	V _{CC} = 5.5 V 1/, V _{IN} = 4.5 V	01	-3	-15	mA
		V _{CC} = 5.5 V 1/	02	-3	-20	mA
		V _{CC} = 5.5 V, V _{OUT} = 0 V 1/	03	-2.5	-25	mA
		V _{CC} = 5.5 V, V _{OUT} = 0 V 1/	04	-2.5	-25	mA
		V _{CC} = 5.5 V, V _{OUT} = 0 V 1/	05	-3	-15	mA
Supply current	I _{CC}	V _{CC} = 5.5 V, V _{IH} = 4.5 V, V _{IL} = 0 2/	01	---	9	mA
		V _{CC} = 5.5 V, V _{IH} = 4.5 V 2/	02	---	27	mA
		V _{CC} = 5.5 V 2/	03		25.3	mA
		V _{CC} = 5.5 V 2/	04		23	mA
		V _{CC} = 5.5 V 2/	05		9	mA

TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions	Device type	Limits		Units
				Min	Max	
Maximum shift frequency	f_{MAX}	$V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, R_L = 4 \text{ k}\Omega$ (see figure 6)	01	3	---	MHz
Propagation delay time, low-to-high level from clock 1 or clock 2 to outputs	t_{PLH}				250	ns
Propagation delay time, high-to-low level from clock 1 or clock 2 to outputs	t_{PHL}				250	ns
Low level setup time at mode control with respect to clock 1 input	t_1			225	---	ns
High level setup time at mode control with respect to clock 2 input	t_2			200	---	ns
Low level setup time at mode control with respect to clock 2 input	t_3			0	---	ns
High level setup time at mode control with respect to clock 1 input	t_4			100	---	ns
Width of clock pulse	t_p	See figure 6	01	200	---	ns
Setup time required at serial A, B, C, D inputs	$t_{SETUP(H)}$	See figure 6	01	100	---	ns
	$t_{SETUP(L)}$				---	ns
Hold time required at serial A, B, C, D inputs	$t_{HOLD(H)}$	See figure 6	01	0	---	ns
	$t_{HOLD(L)}$			0	---	ns
Maximum clock frequency	f_{MAX}	$V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, R_L = 800\Omega$ (figure 7)	02	12	---	MHz
Propagation delay time, high-to-low level, clear input to Q outputs	t_{PHL1}			10	110	ns
Propagation delay time, high-to-low level, clock input to Q outputs	t_{PHL2}			10	100	ns
Propagation delay time, low-to-high level, clock input to Q outputs	t_{PLH2}			10	80	ns
Width of clock or clear pulse	t_p			40	---	ns
Data setup time	$t_{SETUP(H)}$			30	---	ns
	$t_{SETUP(L)}$			30	---	ns
Data hold time	$t_{HOLD(H)}$			0		ns
	$t_{HOLD(L)}$			0		ns

TABLE I. Electrical performance characteristics. - Continued

Test	Symbol	Conditions	Device type	Limits		Units
				Min	Max	
Maximum clock frequency	f_{MAX}	$V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, R_L = 1600\Omega$ (figure 8)	03	6	---	MHz
Propagation delay time, low-to-high level, clock input to Q outputs	t_{PLH1}			11	55	ns
Propagation delay time, high-to-low level, clock input to Q outputs	t_{PHL1}			20	100	ns
Propagation delay, high-to-low level, MR to Q outputs	t_{PHL2}			30	125	ns
Width of clock pulse	t_{P1}			65	20	ns
Width of MR pulse with clock HIGH	t_{P2}			65	20	ns
Width of MR pulse with clock LOW	t_{P3}			75	20	ns
Shift Right frequency	f_{SR}			5	25	MHz
Propagation delay, low-to-high, clock to output	t_{PLH1}			14	100	ns
Propagation delay, high-to-low, clock to output	t_{PHL1}			20	100	ns
Propagation delay, high-to-low, MR to output (except Q3)	t_{PHL2}	$V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, R_L = 1600\Omega$ (figure 9)	04	20	100	ns
Propagation delay, high-to-low, MR to Q3	t_{PHL3}			25	120	ns
Clock pulse width	t_{P1}			20	55	ns
Master reset pulse width	t_{P2}			20	75	ns
Setup time, data to clock	t_{SETUP1}			25	60	ns
Setup time, \overline{PE} to clock	t_{SETUP2}			25	70	ns
Hold time, data to clock	t_{HOLD1}			-40	0	ns
Hold time, \overline{PE} to clock	t_{HOLD2}			-65	-20	ns
Recovery time, \overline{MR} to clock	t_{REC}			20	60	ns
Maximum clock frequency	f_{MAX}			3	---	MHz
Propagation delay time, high-to-low level, clear input to Q outputs	t_{PHL1}	$V_{CC} = 5 \text{ V}, C_L = 50 \text{ pF}, R_L = 800\Omega$ (figure 10)	05	140	ns	
Propagation delay time, high-to-low level, clock input to Q outputs	t_{PHL2}			120	ns	
Propagation delay time, low-to-high level, clock input to Q outputs	t_{PLH2}			120	ns	
Width of clock or clear pulse	t_p			40	---	ns
Data setup time	$t_{SETUP(H)}$			---	60	ns
	$t_{SETUP(L)}$			---	60	ns
Data hold time	$t_{HOLD(H)}$			-10	---	ns
	$t_{HOLD(L)}$			-10	---	ns

1/ Not more than one output should be shorted at a time.

2/ I_{CC} is measured in accordance with Table III requirements.

- (b) Temperature cycling (method 1010 of MIL-STD-883).
 - (1) Omit seal test as post-test measurements.
- (c) Thermal shock (method 1011 of MIL-STD-883), when substituted for temperature cycling.
 - (1) Omit seal test as post-test measurements.
- (d) Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition D or E, using the circuit shown on figure , or equivalent.
 - (2) $T_A = 125^\circ\text{C}$ minimum.
- (e) Reverse bias burn-in and interim electrical test in accordance with 3.1.10 of method 5004 of MIL-STD-883 may be omitted.
- (f) Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- (g) External visual inspection shall not include measurement of case and lead dimensions.
- (h) Percent defective allowable (PDA) - The PDA is specified as 5 percent for class A devices and 10 percent for class B devices based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)		
	Class A devices	Class B devices	Class C devices
Interim electrical parameters (pre burn-in) (method 5004)	1	1	None
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11	1*, 2, 3, 7, 9	1, 7
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9	1, 2, 3, 9
Group C end point electrical parameters (method 5005)	1, 2, 3	1, 2, 3	1
Additional electrical subgroups for group C periodic inspections	None	10, 11	10, 11

*PDA applies to subgroup 1 (see 4.3(h)).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

- (a) Tests shall be as specified in table II.
- (b) Subgroups 4, 5, and 6 of table I of method 5005 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of method 5005 of MIL-STD-883 and as follows:

- (a) Bond strength test may be conducted on samples collected prior to sealing (see 4.3(a)).

4.4.3 Group C inspection. Group C inspection shall consist of the test subgroups and LTPD values shown in table III of method 5005 of MIL-STD-883 and as follows:

- (a) End point electrical parameters shall be as specified in table II.
- (b) Lead bend in only one direction is required for initial conditioning prior to moisture resistance and salt atmosphere tests.
- (c) High temperature storage test (method 1008 of MIL-STD-883) conditions:
 - (1) Temperature: $150^{\circ} \pm 10^{\circ}\text{C}$.
 - (2) Duration: 1,000 hours, except as otherwise permitted by appendix B of MIL-M-38510.
- (d) Operating life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D or E, using the circuit shown on figure , or equivalent.
 - (2) $T_A = 125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510.
- (e) Omit steady-state reverse bias test.
- (f) Subgroups 7 and 8 shall be added to the group C inspection requirements for class B and C devices and shall consist of the tests, conditions, and limits specified for subgroups 10 and 11 of group A.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life-test cooldown procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias. Alternately, the bias may be removed during cooling if the case temperature is reduced to room temperature within 30 minutes after removal of the test condition.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits shall be prepared for delivery in accordance with MIL-M-38510.

6. NOTES

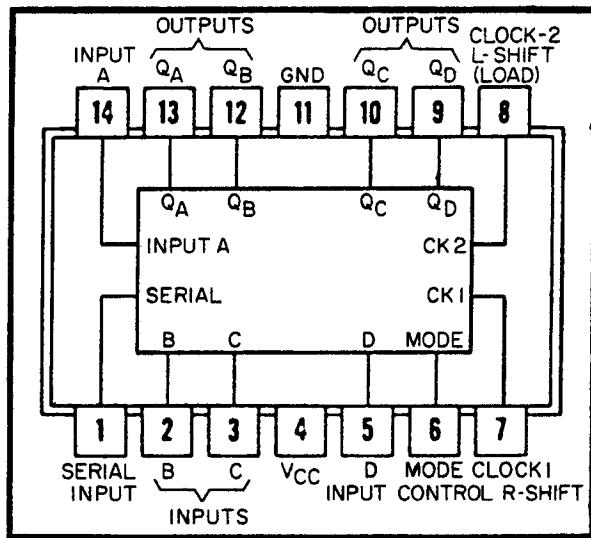
6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic purposes.

6.3 Ordering data. The contract or order should specify the following:

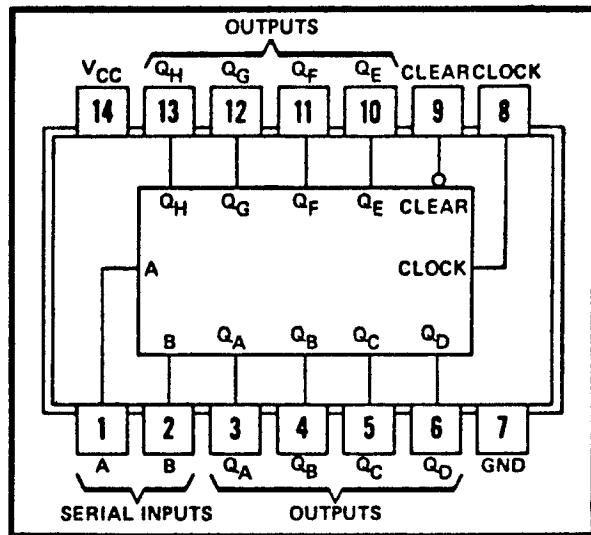
- (a) Complete part number (see 1.2).
- (b) Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

Device type 01



Cases A, B, C, D

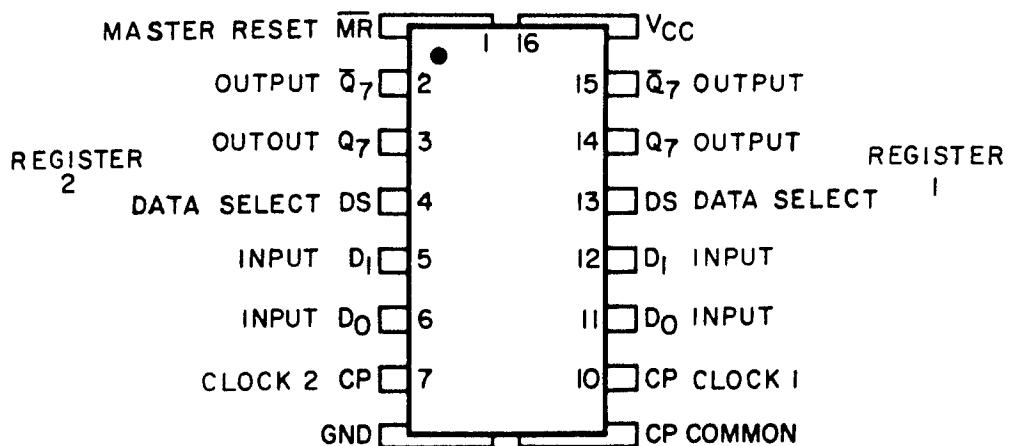
Device types 02, 05



Cases A, B, C, D

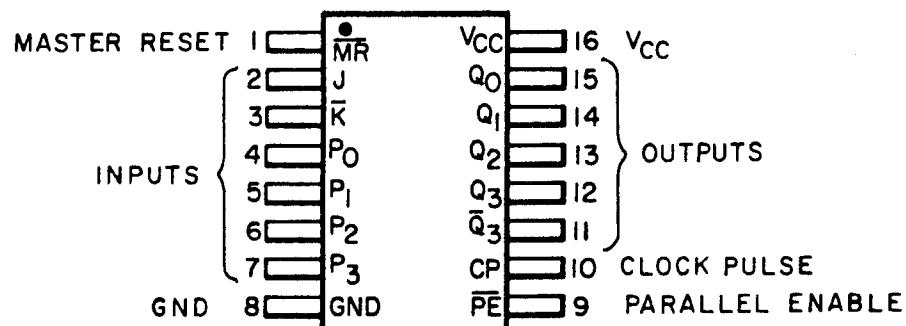
FIGURE 1. Terminal connections.

Device type 03



Cases E, F

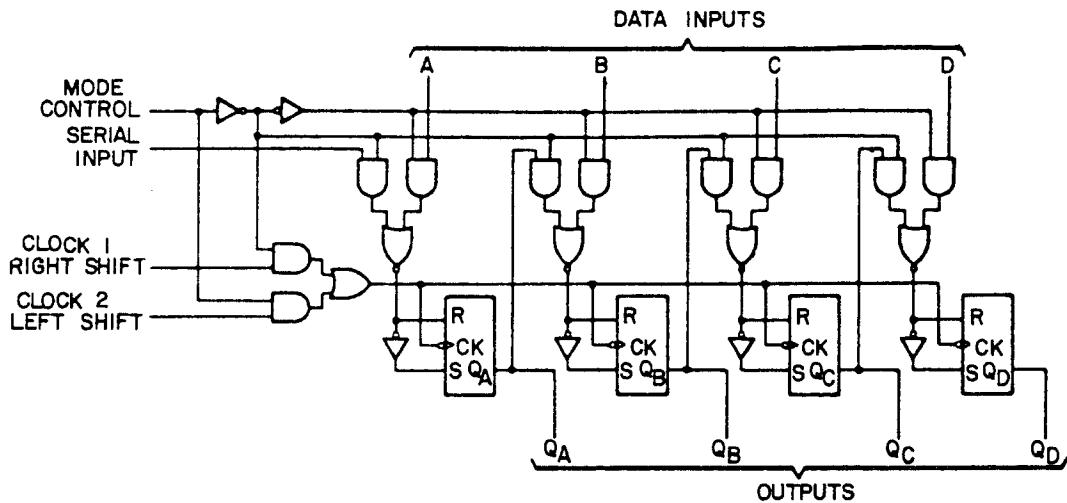
Device type 04



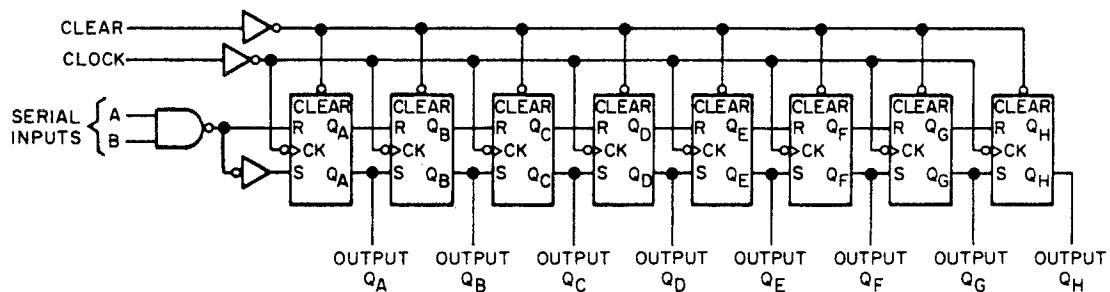
Cases E, F

FIGURE 1. Terminal connections - Continued.

Device type 01



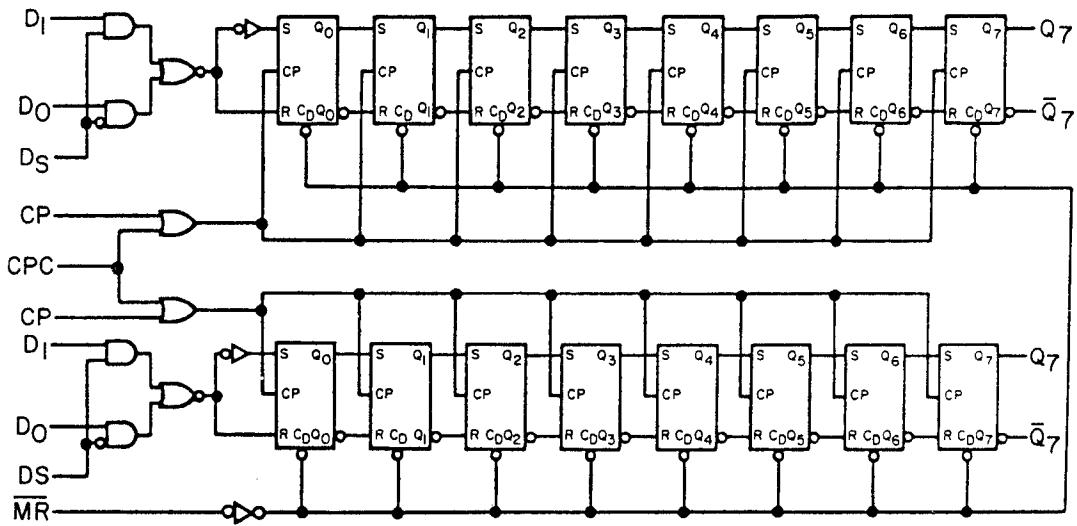
Device types 02, 05



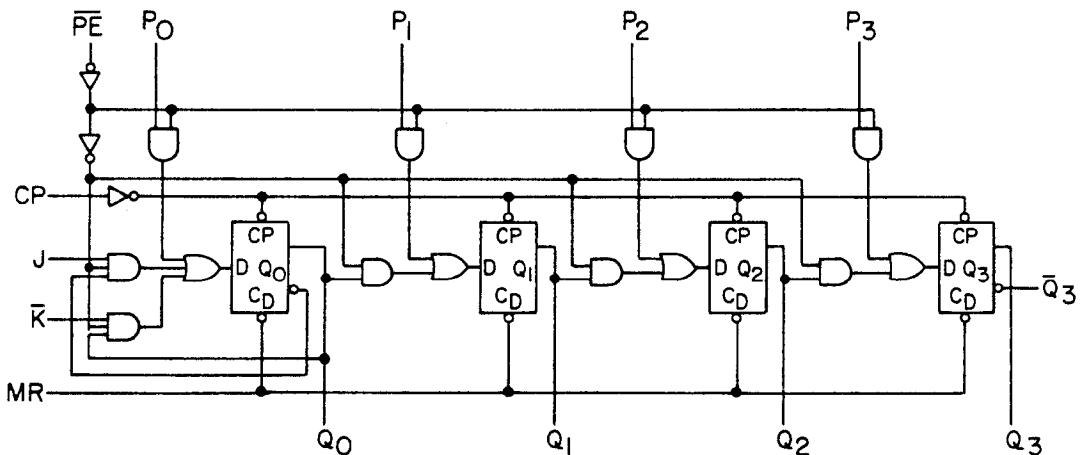
— · · · DYNAMIC INPUT ACTIVATED BY TRANSITION FROM A HIGH LEVEL TO A LOW LEVEL

FIGURE 2. Logic diagram.

Device type 03



Device type 04

FIGURE 2. Logic diagram - Continued.

Device type 01

MODE CONTROL	INPUTS		PARALLEL				OUTPUTS			
	CLOCKS 2(L) 1(R)	SERIAL	A	B	C	D	QA	QB	QC	QD
			X	X	X	X	QAO	QBO	QCO	QDO
H	H	X	X	X	X	X	a	b	c	d
H	↓	X	X	a	b	c	d	a	b	c
H	↓	X	X	QB↑	QC↑	QD↑	d	QBn	QCn	QDn
L	L	H	X	X	X	X	X	QAO	QBO	QCO
L	X	↓	H	X	X	X	X	H	QAn	QBn
L	X	↓	L	X	X	X	X	L	QAn	QBn
↑	L	L	X	X	X	X	X	QAO	QBO	QCO
↓	L	L	X	X	X	X	X	QAO	QBO	QCO
↓	L	H	X	X	X	X	X	QAO	QBO	QCO
↑	H	L	X	X	X	X	X	QAO	QBO	QCO
↑	H	H	X	X	X	X	X	QAO	QBO	QCO

Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C.
 Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant
 (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level.

a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.

QAO, QBO, QCO, QDO = the level of QA, QB, QC, or QD, respectively,
 before the indicated steady state input conditions were established.

QAn, QBn, QCn, QDn = the level of QA, QB, QC, or QD, respectively,
 before the most recent transition of the clock.

FIGURE 3. Truth tables and timing diagrams.

Device types 02 and 05

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	QA	QB	...	QH
L	X	X	X	L	L	...	L
H	L	X	X	QAO	QBO	...	QHO
H	↑	H	H	H	QAn	...	QGn
H	↑	L	X	L	QAn	...	QGn
H	↑	X	L	L	QAn	...	QGn

H = high level (steady state), L = low level (steady state)

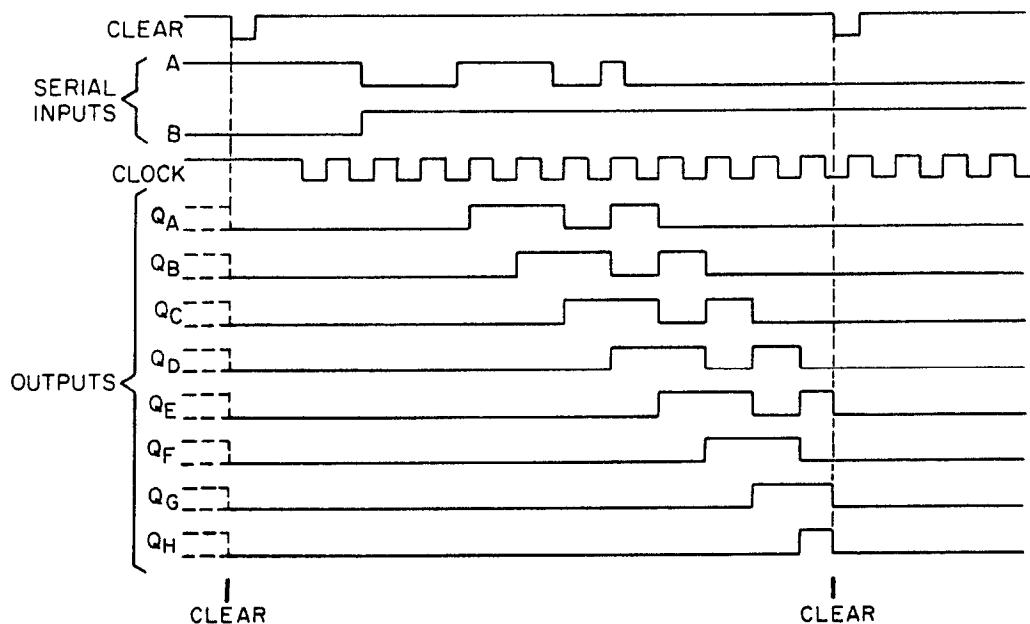
X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

QAO, QBO, QHO = the level of QA, QB, or QH, respectively,
before the indicated steady state input conditions were established.

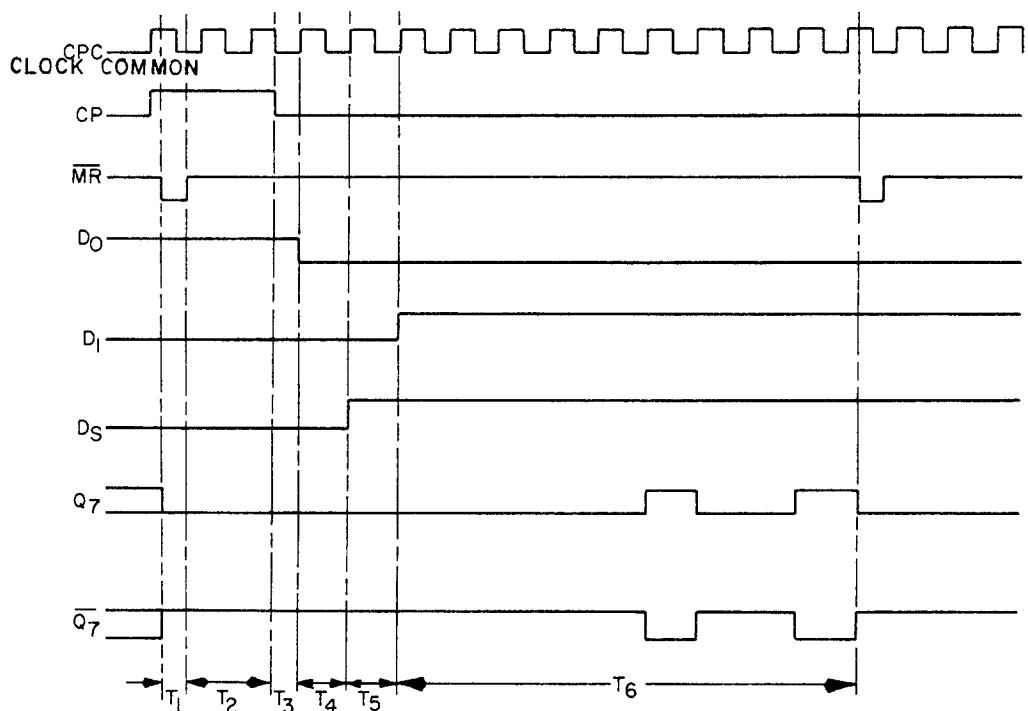
QAn, QGn = the level of QA or QG before the most recent transition
of the clock; indicates a one bit shift.

typical clear, shift, and clear sequences

FIGURE 3. Truth tables and timing diagrams - Continued.

Shift selection			Output
D _S	D _O	D ₁	Q ₇ (t _{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

N+8 = Indicates state after eight clock pulse
 L = Low voltage level
 H = High voltage level
 X = Either high or low voltage level



KEY TO SEQUENCE: -

- | | |
|--|--|
| T ₁ = Clear (MR LOW) | T ₅ = Load logic 'L' via D ₁ |
| T ₂ = Inhibit (CP HIGH) | (D ₁ LOW, D _S HIGH) |
| T ₃ = Load logic 'H' via D _O | T ₆ = Load logic 'H' via D ₁ |
| (D _O HIGH, D _S LOW) | (D ₁ HIGH, D _S HIGH) |
| T ₄ = Load logic 'L' via D _O | |
| (D _O LOW, D _S LOW) | |

Typical clear-inhibit-load-clear sequence.

FIGURE 3. Truth tables and timing diagrams - Continued.

Device type 04

3a. SERIAL ENTRY

 $(\overline{PE} = \text{HIGH}, \overline{MR} = \text{HIGH})$

J	\overline{K}	Q_O at t_{n+1}
L	L	L
L	H	Q_O at t_n (no change)
H	L	Q_O at t_n (toggles)
H	H	H

3b. SERIAL ENTRY

 $(\overline{PE} = \text{HIGH}, \overline{MR} = \text{HIGH})$

J & \overline{K} Connected	Q_O at t_{n+1}
L H	L H

3c. PARALLEL ENTRY

 $(\overline{PE} = \text{LOW}, \overline{MR} = \text{HIGH})$

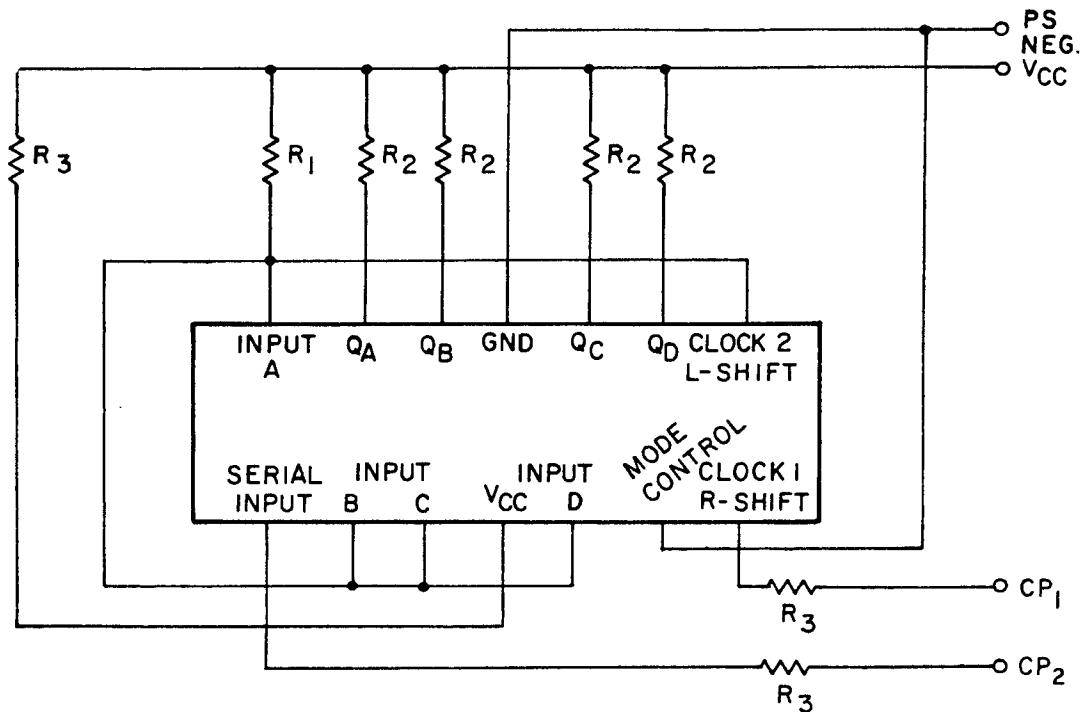
D-Input (P_O, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_O, Q_1, Q_2 or Q_3)
L	L
H	H

 $(n+1 = \text{indicates state after next clock})$

3d. MODE SELECTION

	\overline{PE}	P_O	P_1	P_2	P_3	J	\overline{K}	\overline{MR}
Serial Entry	H	X	X	X	X	Refer to Table 3a & 3b		H
Parallel Entry	L	Refer to Table 3c				X	X	H

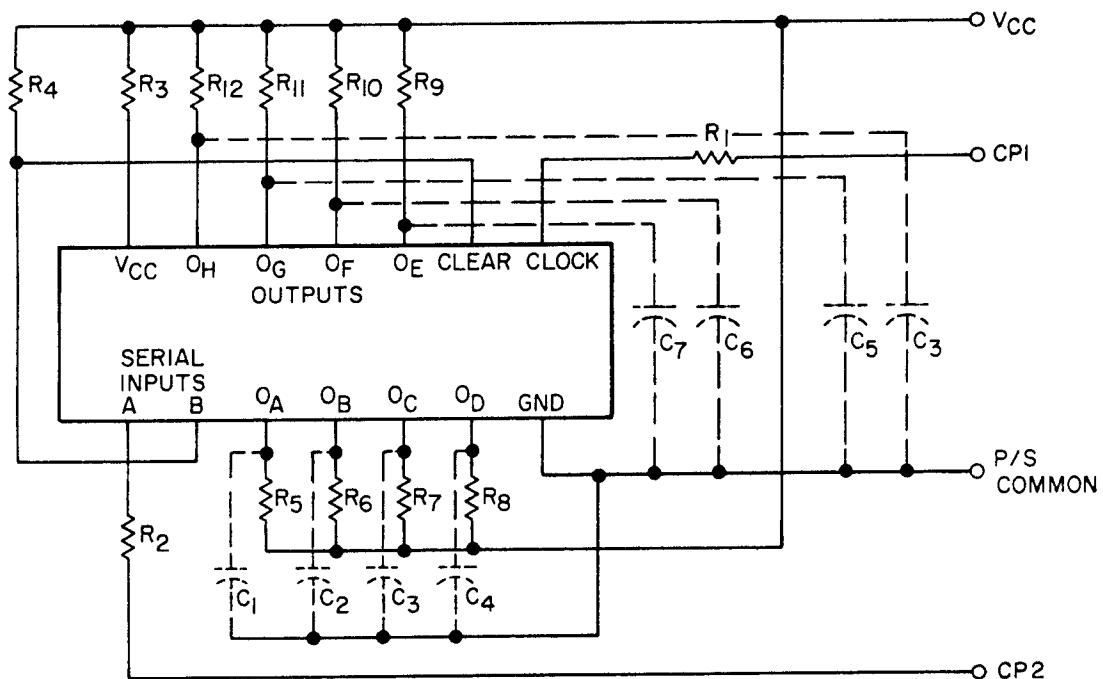
 $H = \text{HIGH voltage level}$ $L = \text{LOW voltage level}$ $X = \text{Don't care}$ FIGURE 3. Truth tables and timing diagrams - Continued.

**NOTES:**

1. V_{CC} shall be of such a value as to provide 5 V min. at device terminals.
2. R₁ = 100Ω ±5%, 1/2 W.
3. R₂ = 2.4 kΩ ±5%, 1/2 W.
4. R₃ = 27Ω ±5%, 1/2 W.
5. CP₁ = 100 kHz, 50% duty cycle, 0-3 V ampl.
6. CP₂ = 50 kHz, 50% duty cycle, 0-3 V ampl.
7. CP₂ voltage transitions shall occur at least 5 ns after CP₁ transitions.

FIGURE 4. Burn-in and life-test circuits.

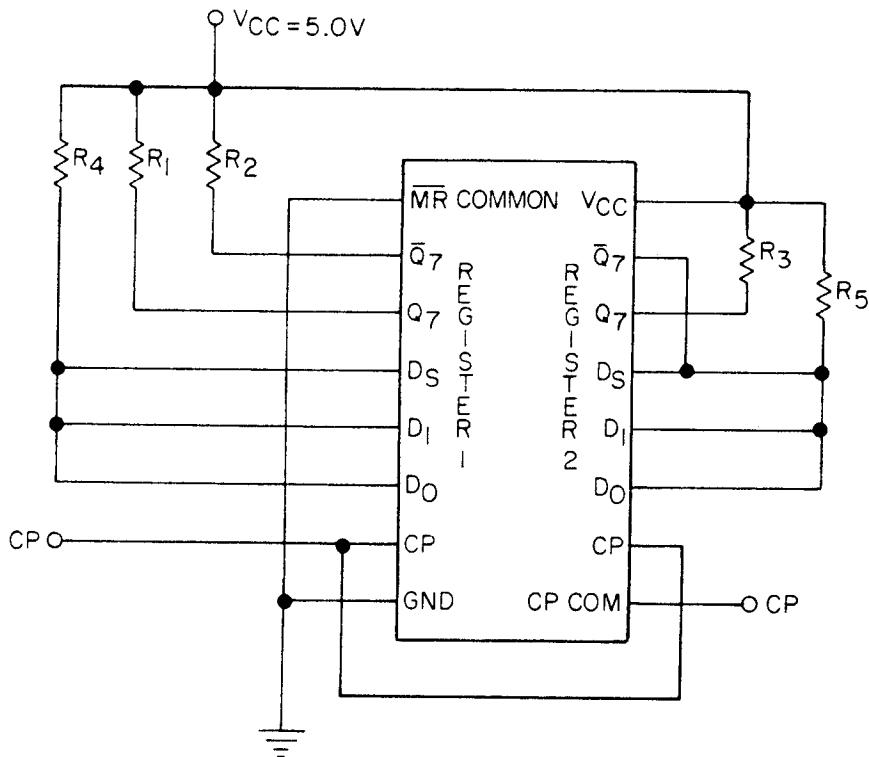
Device type 02



NOTES:

V_{CC} = +5 VR₁, R₂ = 120Ω.R₃ = 4.99Ω.R₄ = 1 kΩ.R₅ → R₁₂ = 1.2 kΩ.C₁ → C₈ = wiring capacitance.CP₁ = 100 kHz, 50% duty cycle, square wave 0-3 V.CP₂ = 50 kHz, 50% duty cycle, square wave 0-3 V.FIGURE 4. Burn-in and life test circuits - Continued.

Device type 03

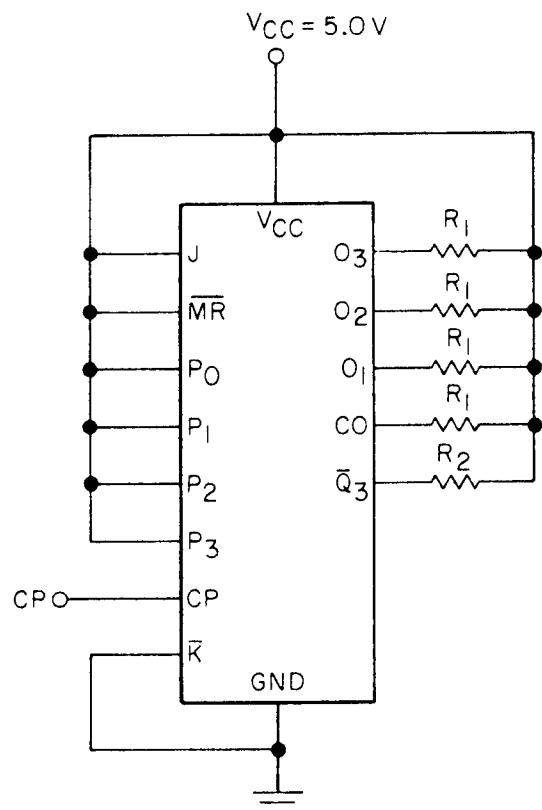


NOTES:

1. R₁ = R₂ = R₃ = 510Ω.
2. R₄ = R₅ = 1 kΩ.
3. CP = 100 kHz, V_{IN} = square wave 0-3 V, 50% duty cycle.

FIGURE 4. Burn-in and life test circuits - Continued.

Device type 04

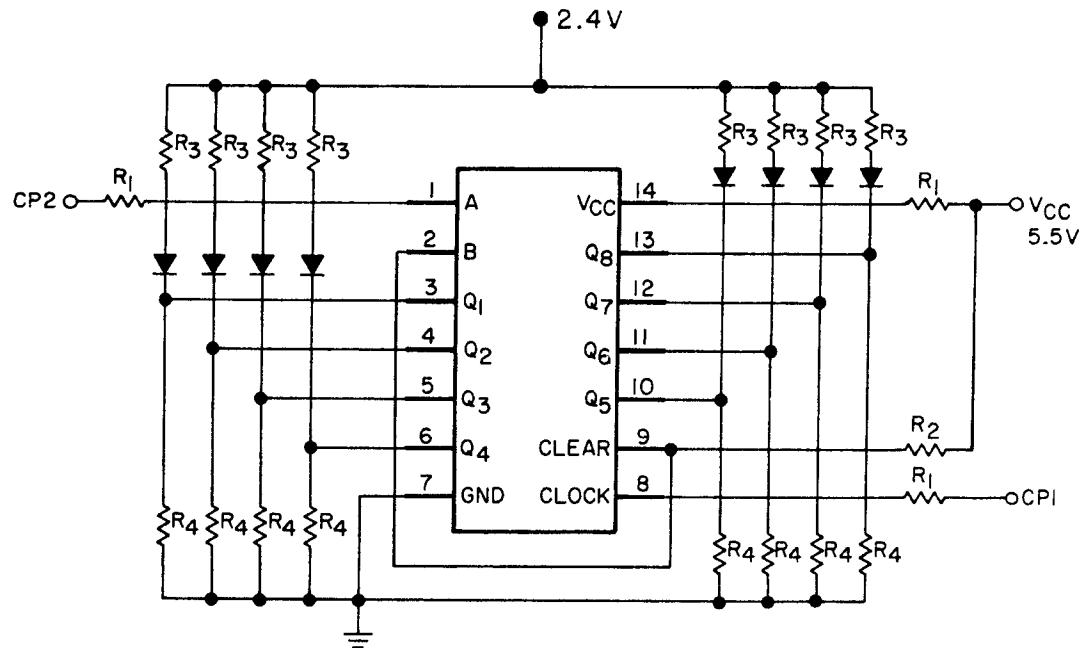


NOTES:

1. $CP = 0-3\text{ V}$
Frequency = 1 MHz
50% duty cycle, min.
2. $R_1 = 470\Omega$.
3. $R_2 = 330\Omega$.

FIGURE 4. Burn-in and life test circuits - Continued.

Device type 05

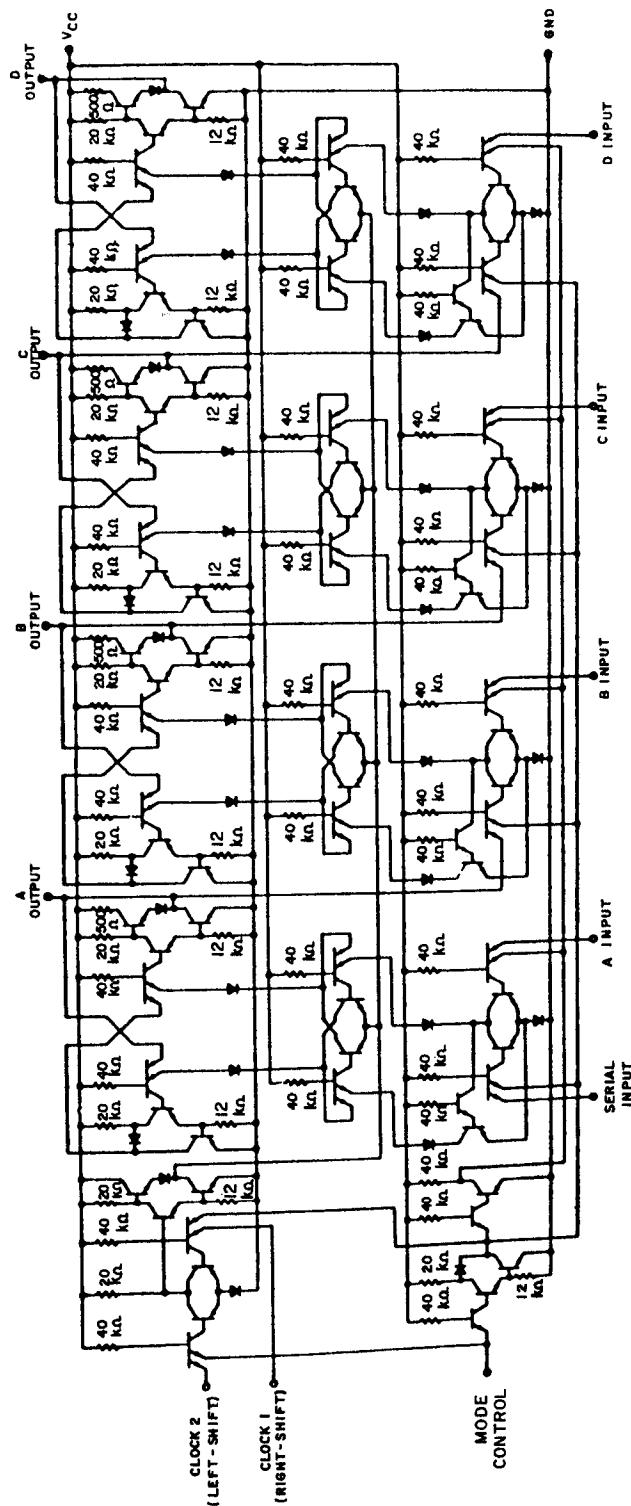


NOTES:

1. $R_1 = 51\Omega$; $R_2 = 1\text{ k}\Omega$; $R_3 = 680\Omega$; $R_4 = 12\text{ k}\Omega$.
2. $CP_1 = 100\text{ kHz}$, 50% duty cycle, 3 V.
3. $CP_2 = 50\text{ kHz}$, 50% duty cycle, 3 V.
4. Diodes are 1N3064 or equivalent.

FIGURE 4. Burn-in and life test circuits - Continued.

Device type 01



NOTE: Component values shown are nominal.

Circuit A

FIGURE 5. Schematic circuit.

Device type 01

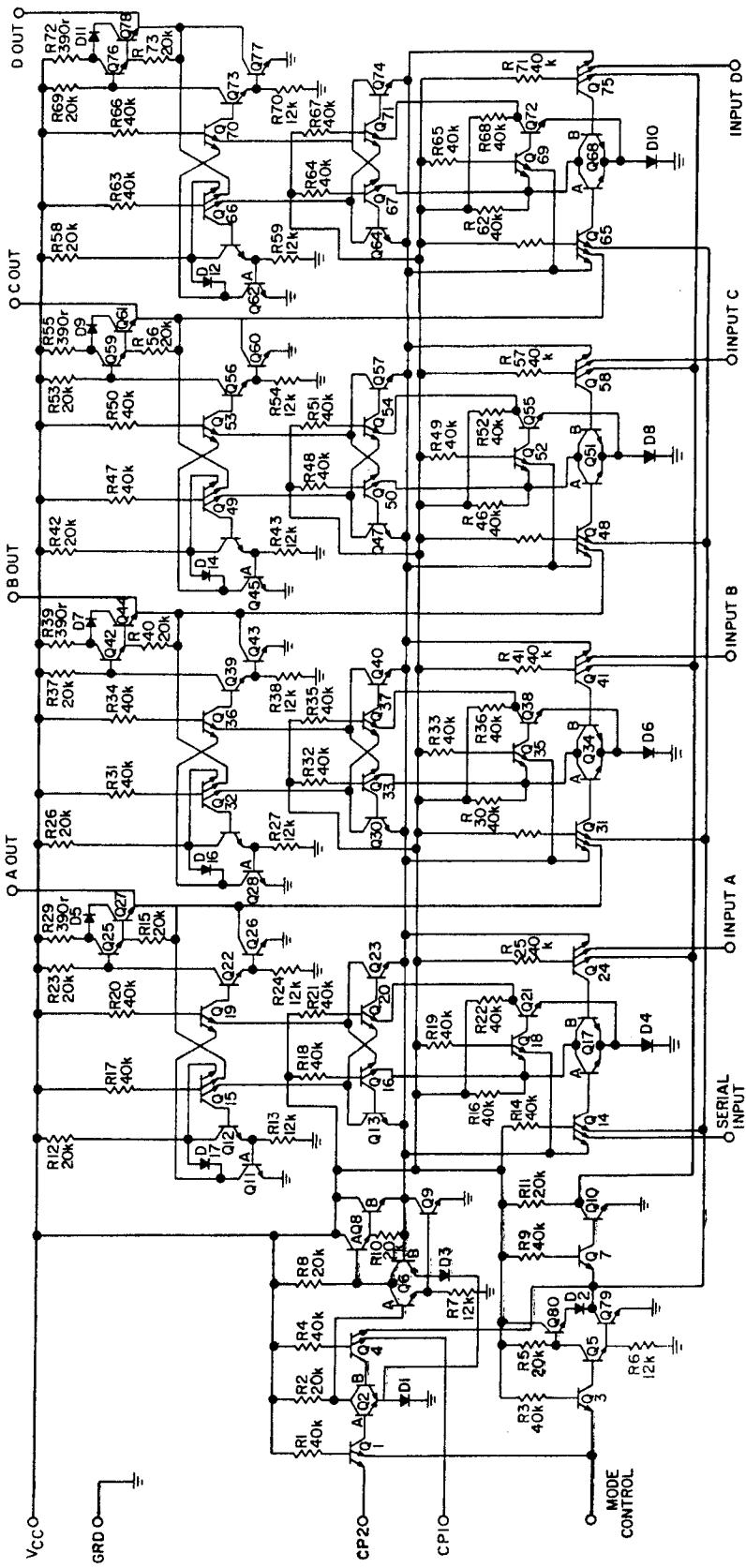


FIGURE 5. Schematic circuit - Continued.

NOTE: Component values shown are nominal.

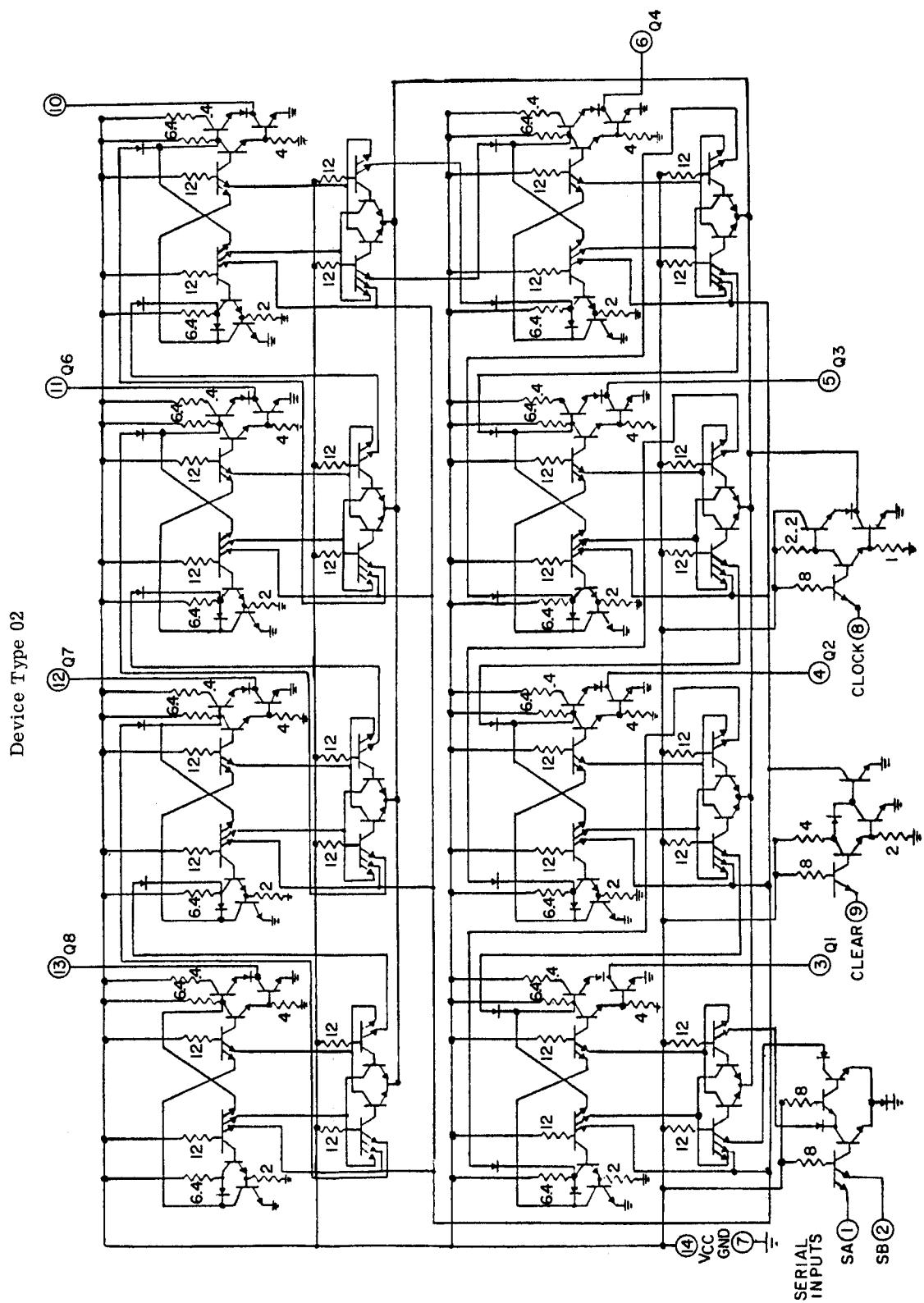
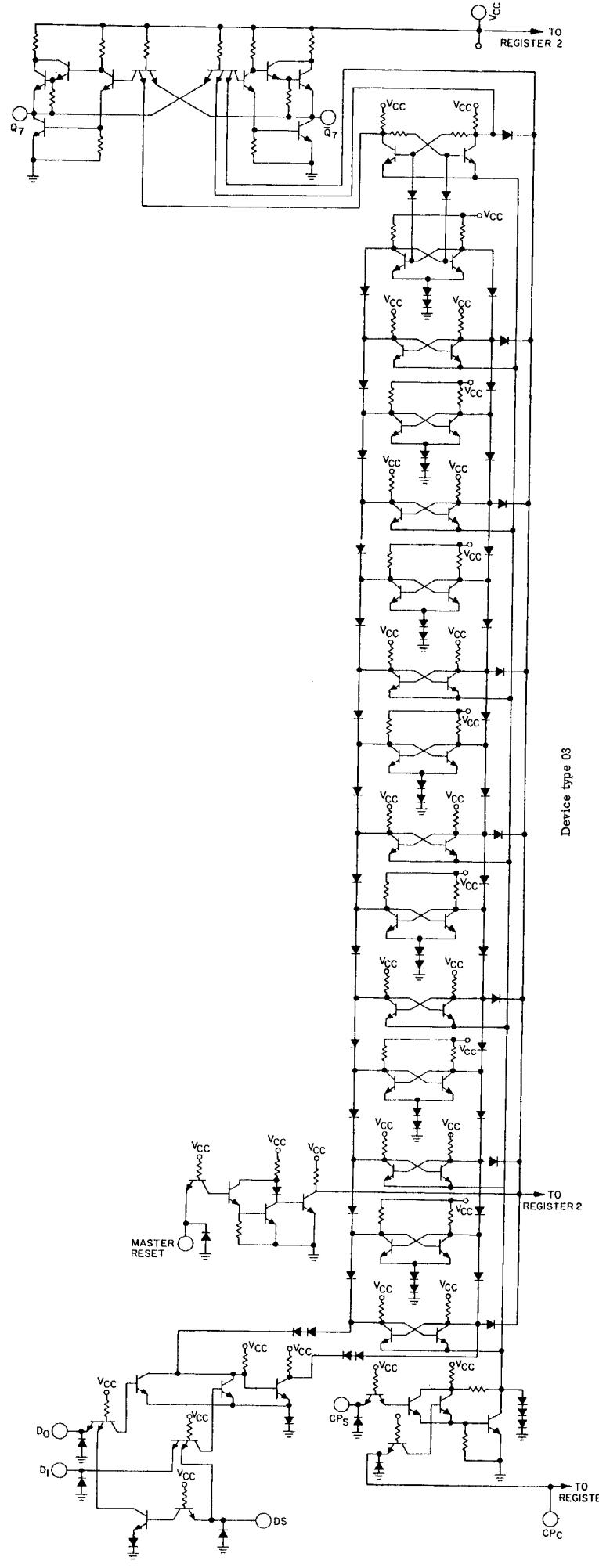
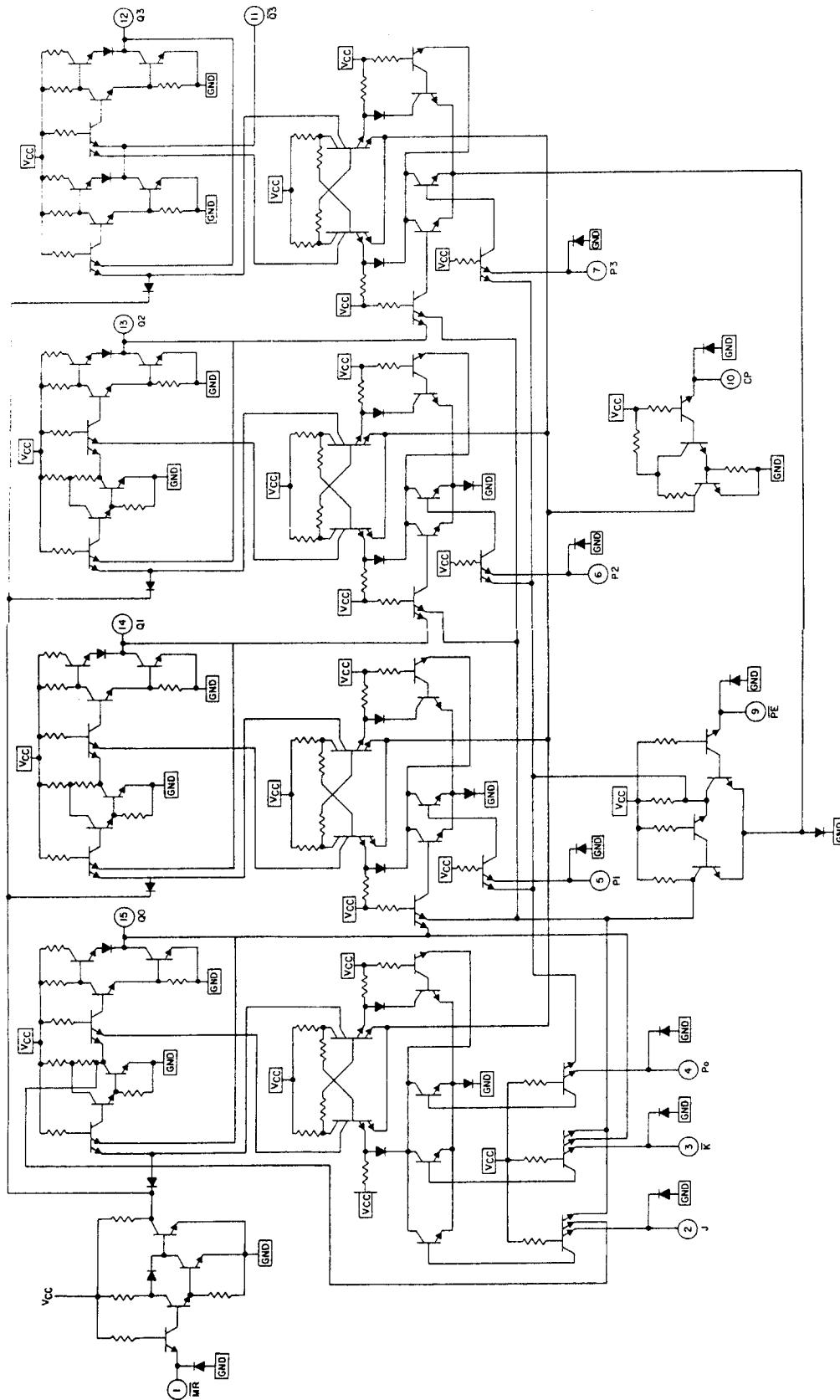


FIGURE 5. Schematic circuit - Continued.



Device type 03

FIGURE 5. Schematic diagram - Continued.



Device type 04

FIGURE 5. Schematic diagram - Continued.

Device type 05

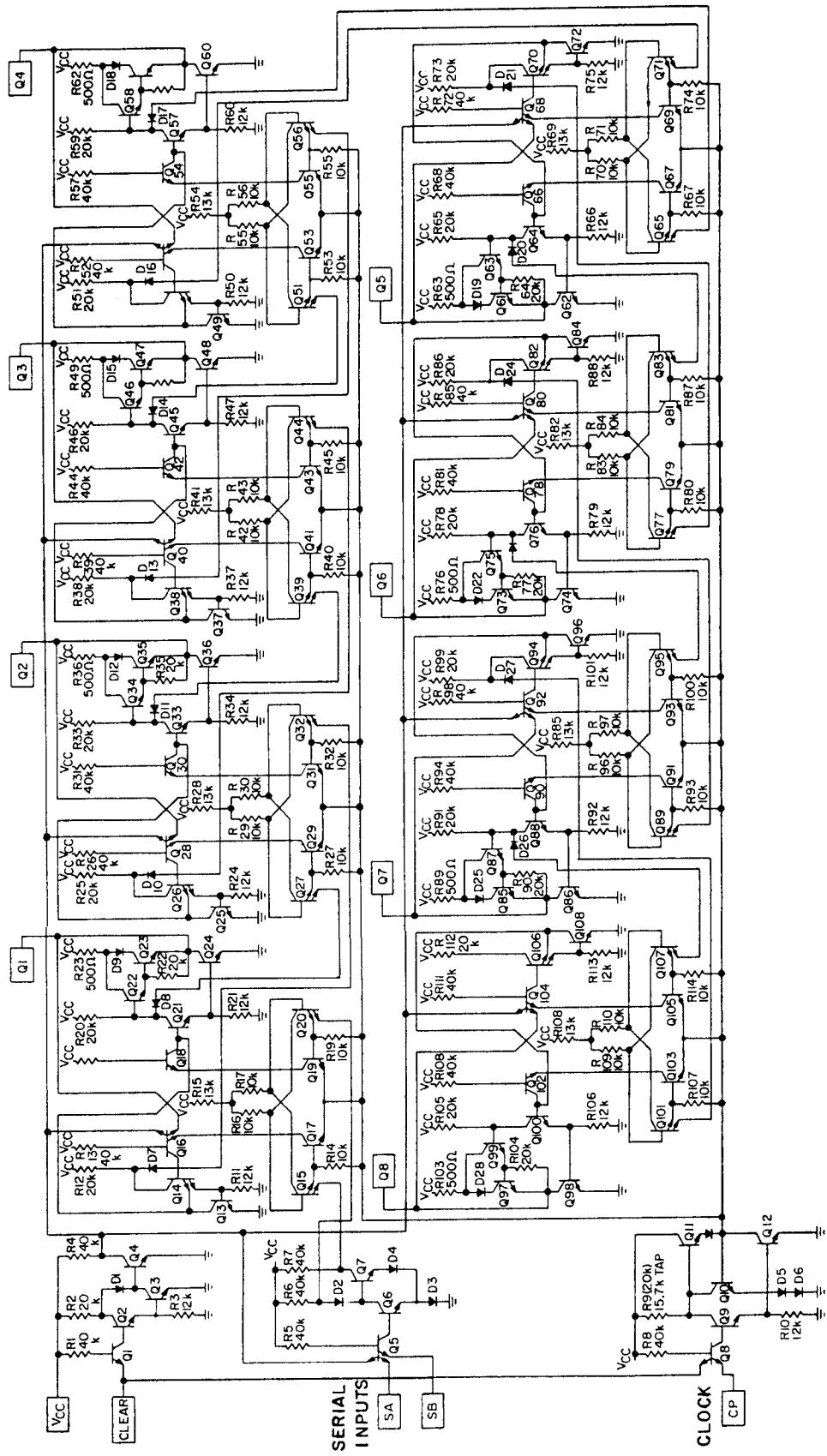
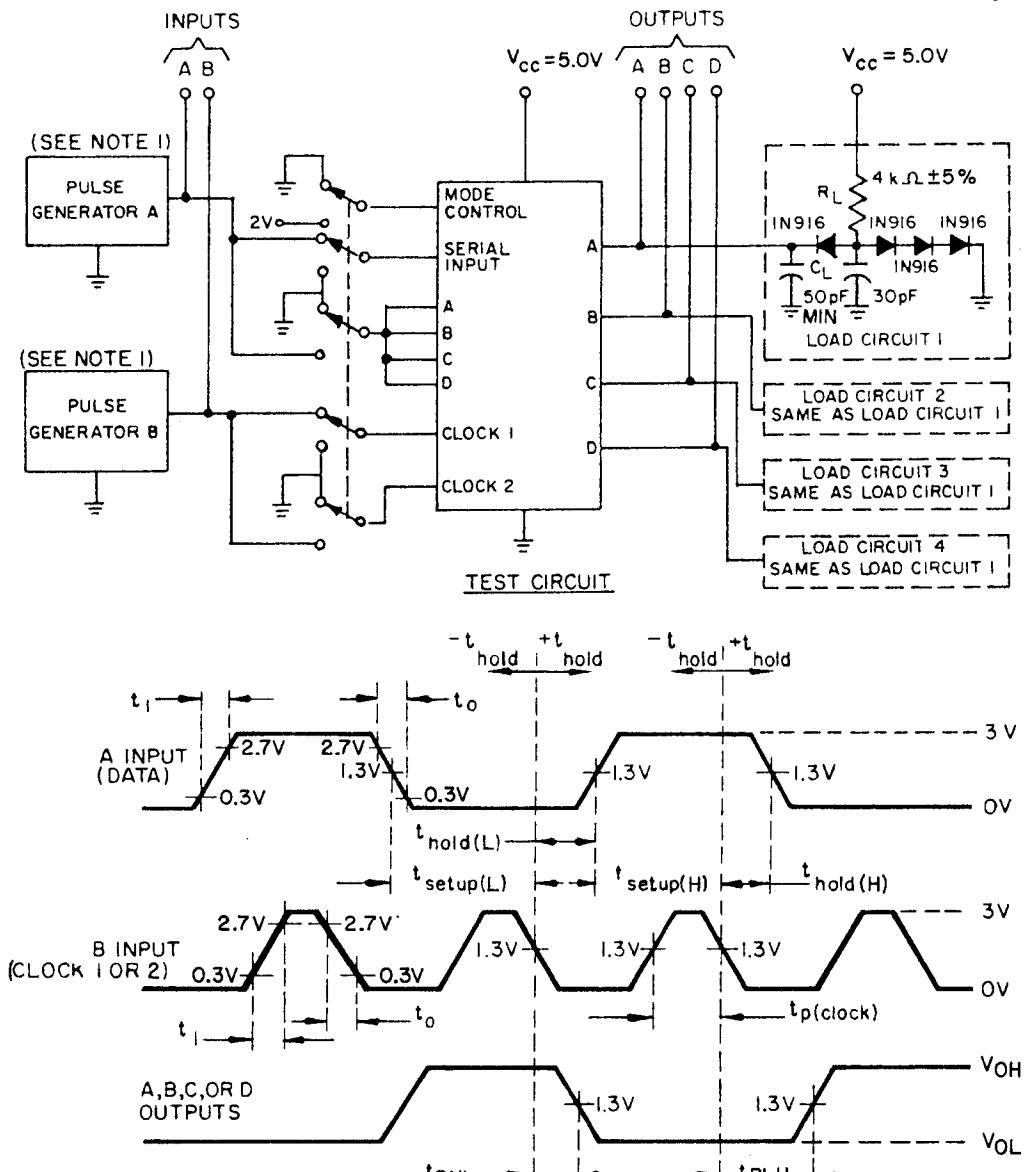
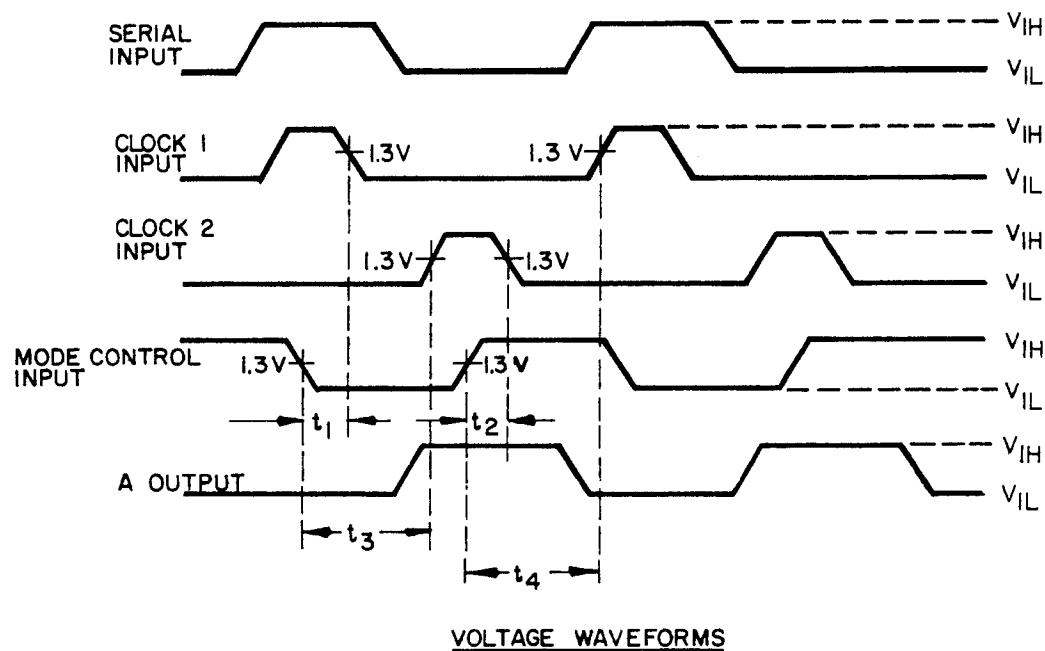


FIGURE 5. Schematic circuit - Continued.

**NOTES:**

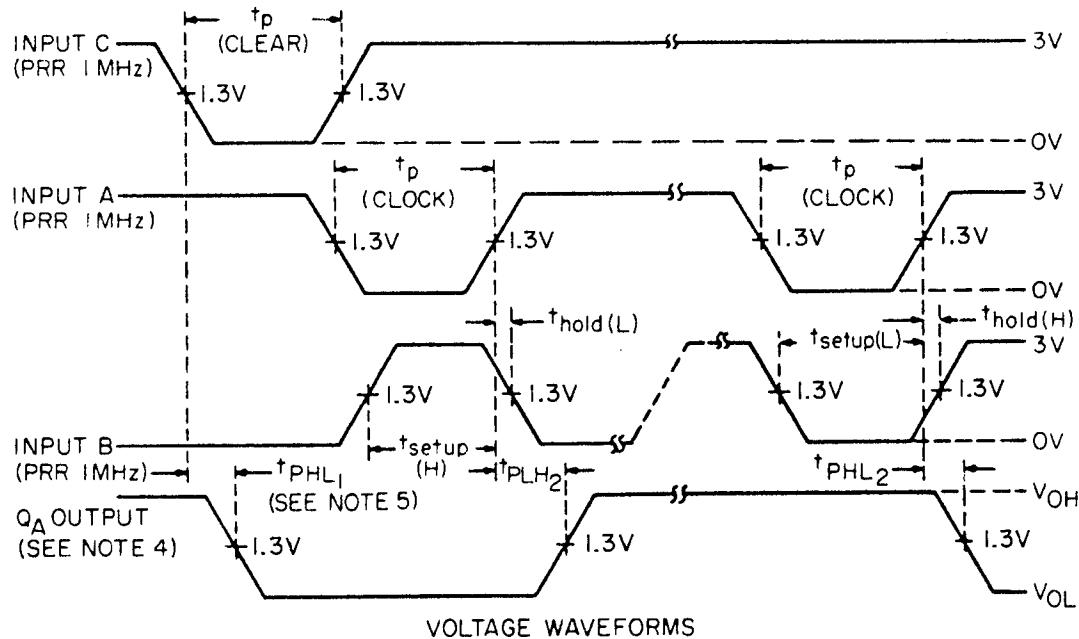
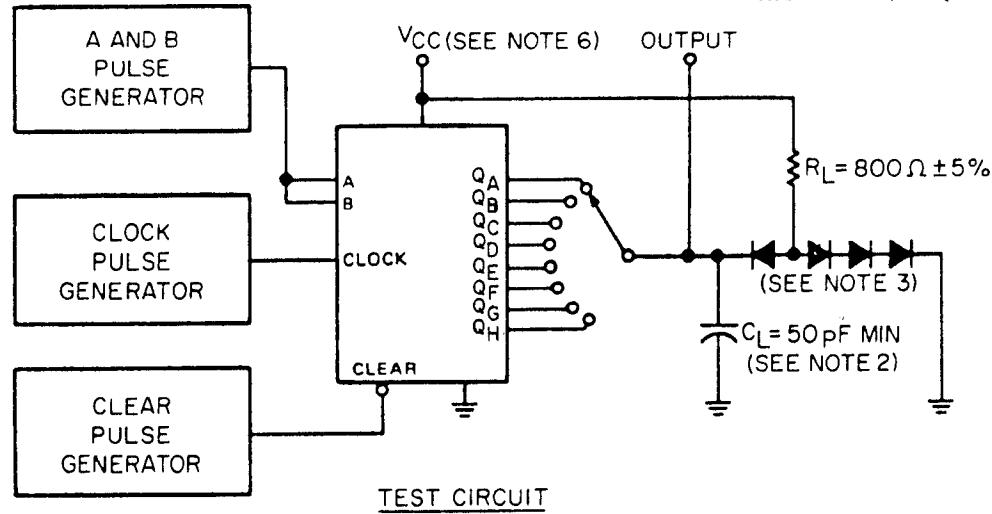
1. The pulse generators have the following characteristics:
 $t_1 \leq 15$ ns, $t_0 \leq 10$ ns, and $Z_{out} \approx 50\Omega$. For pulse generator A: $t_p > 150$ ns and PRR < 500 kHz. For pulse generator B: $t_p > 10$ ns and PRR < 1 MHz. When testing f_{max} , vary PRR.
2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 6. Switching test circuits, waveforms, and mode control setup times for device type 01.



NOTE: A input is at V_{IL} .

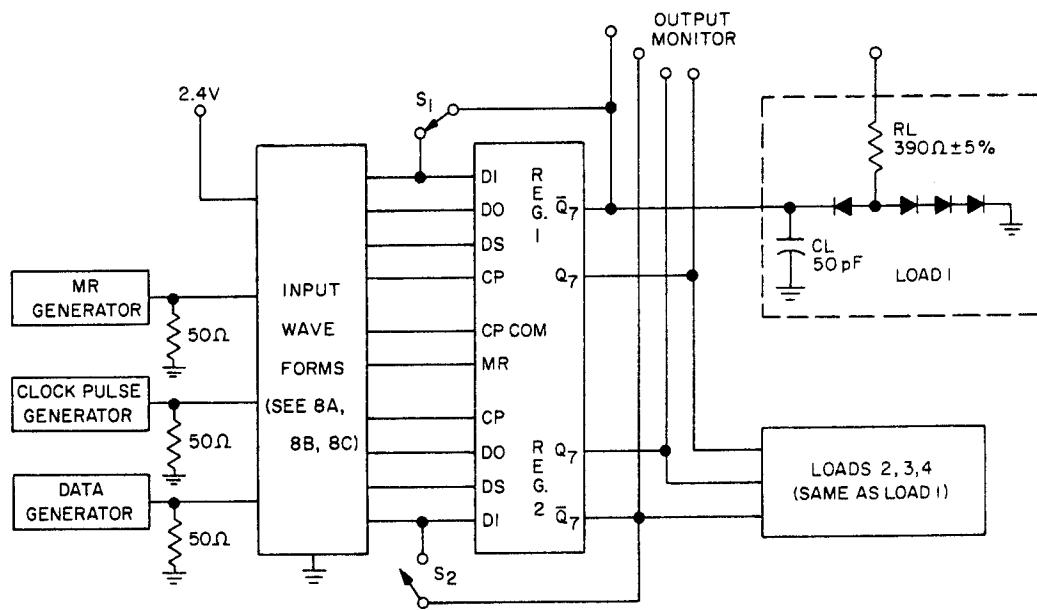
FIGURE 6. Switching test circuits, waveforms, and mode control setup times for device type 01 - Continued.



NOTES:

1. The pulse generators have the following characteristics: $t_r < 10 \text{ ns}$, $t_f < 10 \text{ ns}$, duty cycle $< 50\%$, $Z_{out} \approx 50\Omega$.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N916 or equivalent.
4. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
5. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
6. V_{CC} shall be of sufficient amplitude to provide 5 V at device terminal.

FIGURE 7. Switching test circuits and waveforms for device type 02.



NOTES:

1. C_L includes probe and jig capacitance.
2. All diodes are 1N3064 or equivalent.

FIGURE 8. Switching test circuit and waveforms for device type 03.

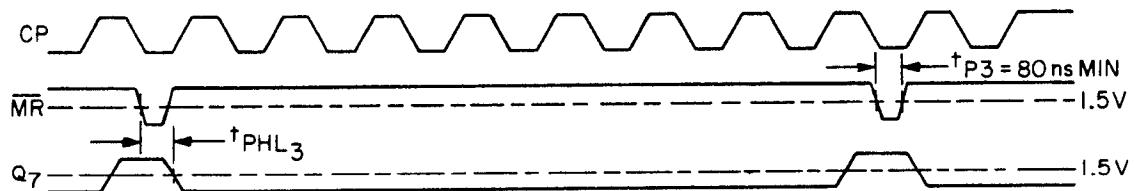
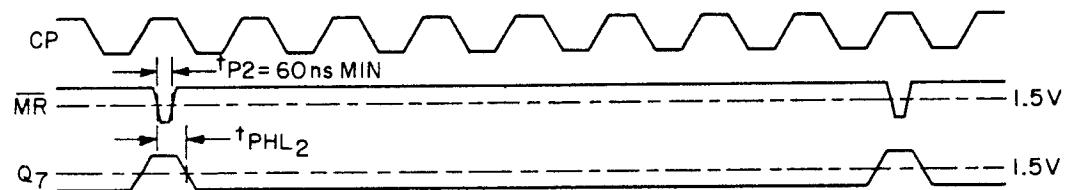
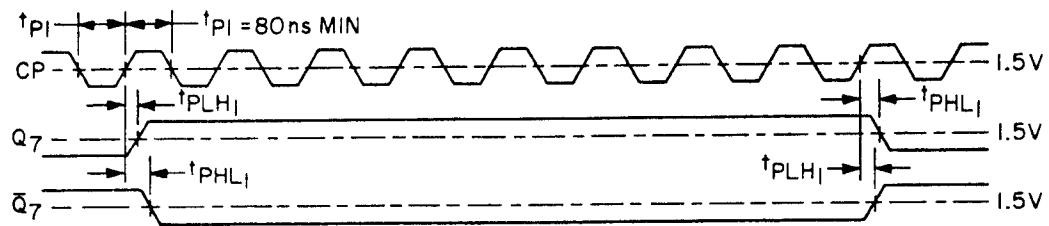
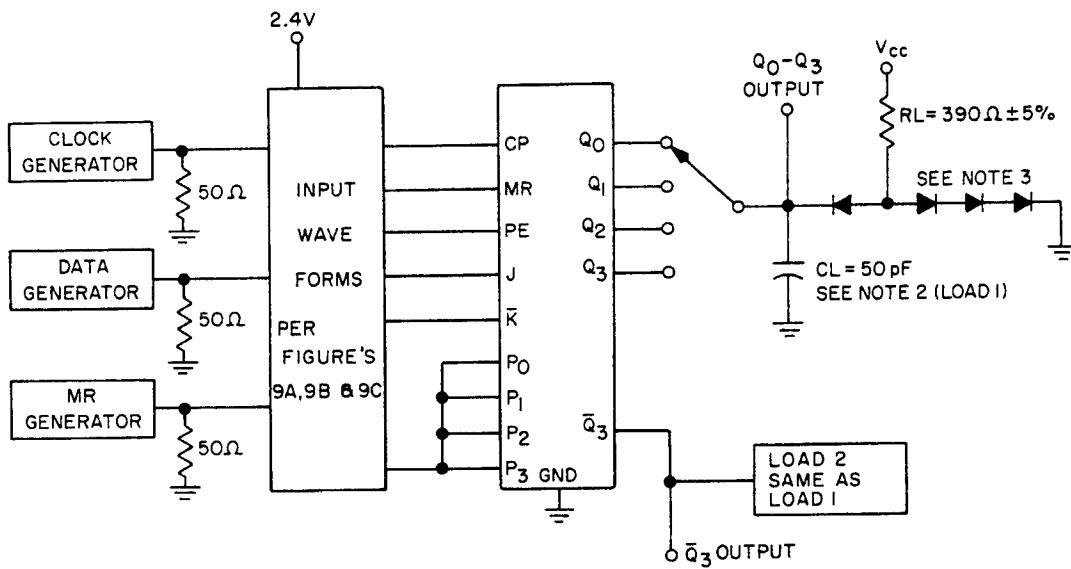


FIGURE 8. Switching test circuit and waveforms for device type 03 - Continued.



NOTES:

1. Generator rise and fall times (measured from 10% to 90% points) are < 5 ns.
2. CL includes probe and jig capacitance.
3. All diodes are 1N3064 or equivalent.
4. Monitor Q₃ loaded when performing f_{SR} test.

FIGURE 9. Switching test circuit and waveforms for device type 04.

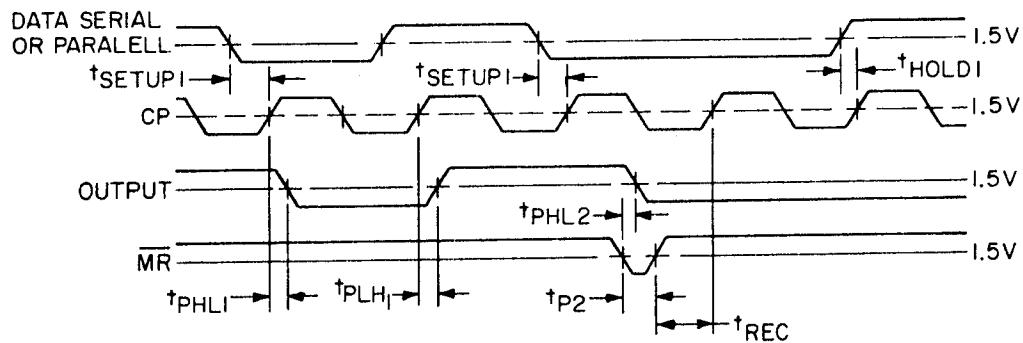


FIGURE 9a.

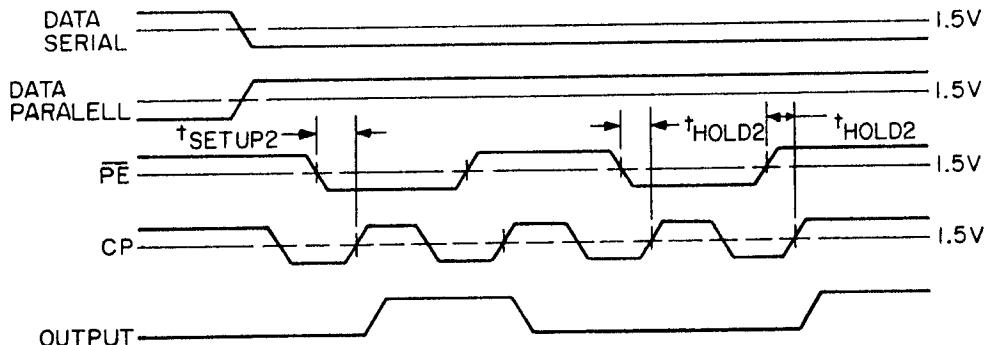


FIGURE 9b.

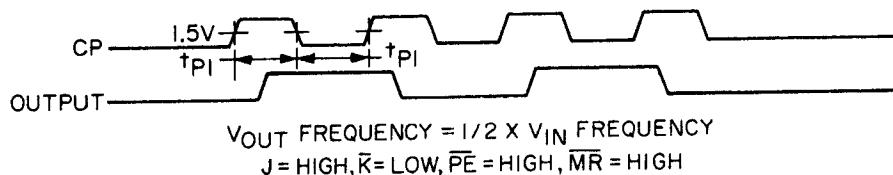
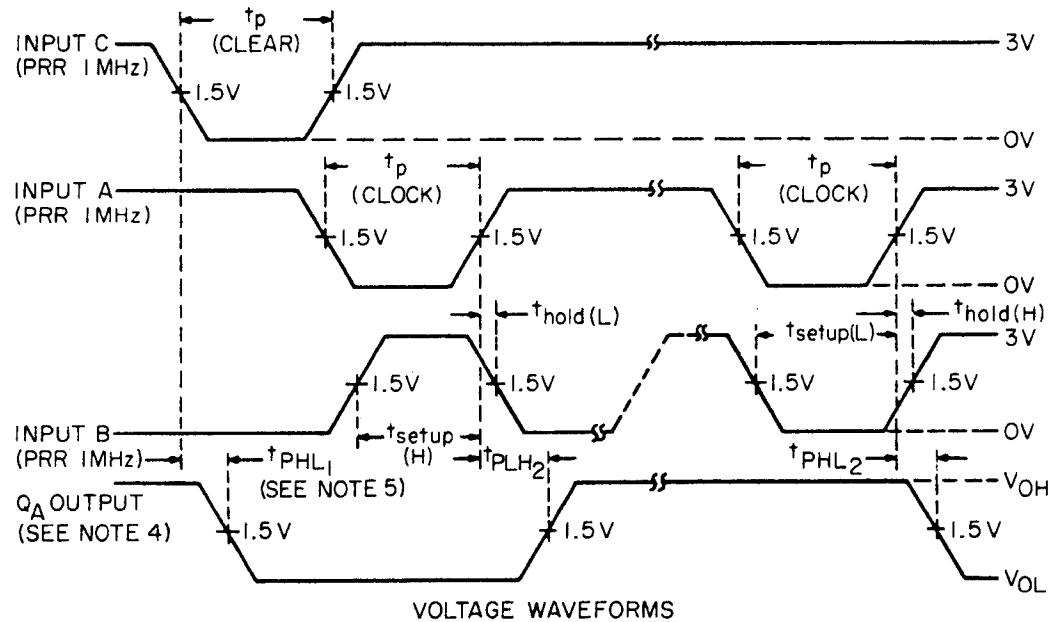
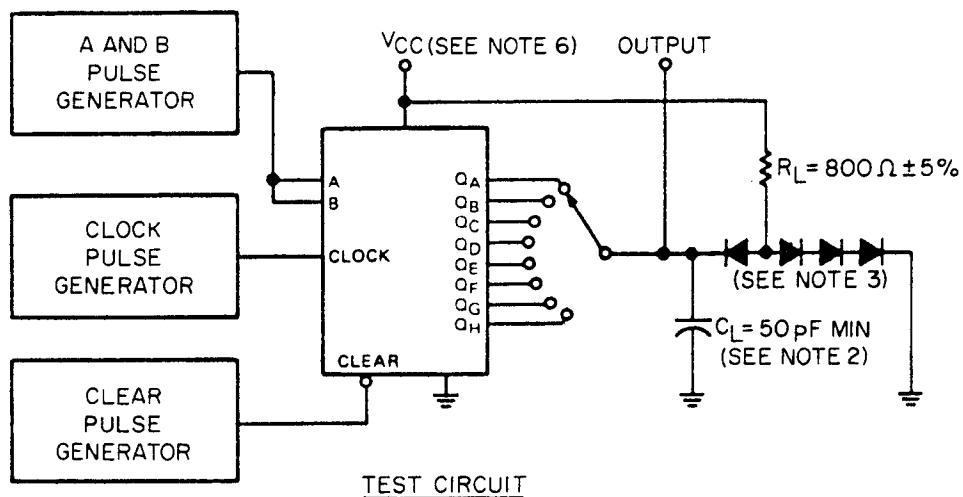


FIGURE 9c.

FIGURE 9. Switching test circuit and waveforms for device type 04 - Continued.

**NOTES:**

1. The pulse generators have the following characteristics: $t_r < 15 \text{ ns}$, $t_f < 15 \text{ ns}$, duty cycle $< 50\%$, $Z_{out} \approx 50\Omega$.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N916 or equivalent.
4. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
5. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
6. V_{CC} shall be of sufficient amplitude to provide 5 V at device terminal.

FIGURE 10. Switching test circuits and waveforms for device type 05.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL- STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits
			Cases serial	Input β	Input β	Input V_{CC}	Input D	Mode control	Clock 1	Clock 2	Output C	Output D	Output GND	Output B	Output A	Input A	Meas. terminal	
$T_A = 25^\circ C$	V _{OH}	3006	1	2.0 V	2.0 V	4.5 V	2.0 V	2.0 V	C	C	-1 mA	-1 mA	2.0 V	OUT A	OUT B	OUT C	OUT D	2.4 V
	V _{OL}	3007	2	2.0 V	0.7 V	0.7 V	0.7 V	0.7 V	C	C	-1 mA	-1 mA	0.7 V	OUT A	OUT B	OUT C	OUT D	0.3 V
	I _{IL1}	3009	3	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	C	C	2 mA	2 mA	0.7 V	OUT A	OUT B	OUT C	OUT D	0.3 V
	I _{IL2}	3009	4	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	C	C	2 mA	2 mA	0.7 V	OUT A	OUT B	OUT C	OUT D	0.3 V
	I _{IH1}	3010	5	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V	C	C	2 mA	2 mA	0.7 V	OUT A	OUT B	OUT C	OUT D	0.3 V
	I _{IH2}	3010	6	0.3 V	0.3 V	0.3 V	0.3 V	0.3 V	GND	GND	0.3 V	0.3 V	0.3 V	IN. ser.	IN. ser.	IN. ser.	IN. ser.	-0.06 to 0.18 mA
	I _{IH3}	3010	7	0.3 V	0.3 V	0.3 V	0.3 V	0.3 V	GND	GND	0.3 V	0.3 V	0.3 V	IN. ser.	IN. ser.	IN. ser.	IN. ser.	-0.12 to 0.36 mA
	I _{TH4}	3010	8	0.3 V	0.3 V	0.3 V	0.3 V	0.3 V	GND	GND	0.3 V	0.3 V	0.3 V	IN. ser.	IN. ser.	IN. ser.	IN. ser.	10 μA
	I _{OS}	3011	9	0.3 V	0.3 V	0.3 V	0.3 V	0.3 V	GND	GND	0.3 V	0.3 V	0.3 V	IN. ser.	IN. ser.	IN. ser.	IN. ser.	2.4 V
	I _{CC}	3005	10	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	GND	GND	0.8 V	0.8 V	0.8 V	IN. ser.	IN. ser.	IN. ser.	IN. ser.	100
	2																	
	3																	
	Same tests, terminal conditions, and limits as for subgroup 1, except $T_A = 125^\circ C$.																	
	$T_A = 72/25^\circ C$																	
	Same tests, terminal conditions, and limits as for subgroup 1, except $T_A = -55^\circ C$.																	

TABLE III. Group A inspection for device type 01. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Terminal conditions (pins not designated as open)												Test limits																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																		
			Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Input A	Output B	Output C	GND	Output D	Clock 2	Clock 1	Mode control	Input 0	Input C	V _{CC}	Input B	Input serial	Test No.	Cases A, B, C, D																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
7 2/ $T_A = 25^\circ C$			A	B	3/	B	3/	4.5	V	B	A	B	B	B	B	B	A	B	B	B	B	B	B	B	B	45	A	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	8010	8011	8012	8013	8014	8015	8016	8017	8018	8019	8020	8021	8022	8023	8024	8025	8026	8027	8028	8029	8030	8031	8032	8033	8034	8035	8036	8037	8038	8039	8040	8041	8042	8043	8044	8045	8046	8047	8048	8049	8050	8051	8052	8053	8054	8055	8056	8057	8058	8059	8060	8061	8062	8063	8064	8065	8066	8067	8068	8069	8070	8071	8072	8073	8074	8075	8076	8077	8078	8079	8080	8081	8082	8083	8084	8085	8086	8087	8088	8089	8090	8091	8092	8093	8094	8095	8096	8097	8098	8099	80100	80101	80102	80103	80104	80105	80106	80107	80108	80109	80110	80111	80112	80113	80114	80115	80116	80117	80118	80119	80120	80121	80122	80123	80124	80125	80126	80127	80128	80129	80130	80131	80132	80133	80134	80135	80136	80137	80138	80139	80140	80141	80142	80143	80144	80145	80146	80147	80148	80149	80150	80151	80152	80153	80154	80155	80156	80157	80158	80159	80160	80161	80162	80163	80164	80165	80166	80167	80168	80169	80170	80171	80172	80173	80174	80175	80176	80177	80178	80179	80180	80181	80182	80183	80184	80185	80186	80187	80188	80189	80190	80191	80192	80193	80194	80195	80196	80197	80198	80199	80200	80201	80202	80203	80204	80205	80206	80207	80208	80209	80210	80211	80212	80213	80214	80215	80216	80217	80218	80219	80220	80221	80222	80223	80224	80225	80226	80227	80228	80229	80230	80231	80232	80233	80234	80235	80236	80237	80238	80239	80240	80241	80242	80243	80244	80245	80246	80247	80248	80249	80250	80251	80252	80253	80254	80255	80256	80257	80258	80259	80260	80261	80262	80263	80264	80265	80266	80267	80268	80269	80270	80271	80272	80273	80274	80275	80276	80277	80278	80279	80280	80281	80282	80283	80284	80285	80286	80287	80288	80289	80290	80291	80292	80293	80294	80295	80296	80297	80298	80299	80300	80301	80302	80303	80304	80305	80306	80307	80308	80309	80310	80311	80312	80313	80314	80315	80316	80317	80318	80319	80320	80321	80322	80323	80324	80325	80326	80327	80328	80329	80330	80331	80332	80333	80334	80335	80336	80337	80338	80339	80340	80341	80342	80343	80344	80345	80346	80347	80348	80349	80350	80351	80352	80353	80354	80355	80356	80357	80358	80359	80360	80361	80362	80363	80364	80365	80366	80367	80368	80369	80370	80371	80372	80373	80374	80375	80376	80377	80378	80379	80380	80381	80382	80383	80384	80385	80386	80387	80388	80389	80390	80391	80392	80393	80394	80395	80396	80397	80398	80399	80400	80401	80402	80403	80404	80405	80406	80407	80408	80409	80410	80411	80412	80413	80414	80415	80416	80417	80418	80419	80420	80421	80422	80423	80424	80425	80426	80427	80428	80429	80430	80431	80432	80433	80434	80435	80436	80437	80438	80439	80440	80441	80442	80443	80444	80445	80446	80447	80448	80449	80450	80451	80452	80453	80454	80455	80456	80457	80458	80459	80460	80461	80462	80463	80464	80465	80466	80467	80468	80469	80470	80471	80472	80473	80474	80475	80476	80477	80478	80479	80480	80481	80482	80483	80484	80485	80486	80487	80488	80489	80490	80491	80492	80493	80494	80495	80496	80497	80498	80499	80500	80501	80502	80503	80504	80505	80506	80507	80508	80509	80510	80511	80512	80513	80514	80515	80516	80517	80518	80519	80520	80521	80522	80523	80524	80525	80526	80527	80528	80529	80530	80

See footnotes at end of table.

TABLE III. Group A inspection for device type 91. - Continued
Terminal conditions (pins not designated are open)

TABLE III. Group A inspection for device type 01. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL- STD-883 Method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits	
		Test No.	Input serial	Input B	Input C	V _{CC}	Input D	Mode control	Clock 1	Clock 2	Output D	Output C	GND	Output B	Output A	Meas. terminal	Min	Max	Unit
10 $T_A = 125^\circ\text{C}$	t_{PHL}	3003 (Fig 6)	121	GND	D	5.0 V	D	2.4 V	GND	C	OUT	OUT	GND	GND	D	CLK 2 to OUT C	250	ns	
11			122	GND	D	5.0 V	D	2.4 V	GND	C	OUT	OUT	GND	GND	D	CLK 2 to OUT D	250	ns	

NOTES: C = Clock pulse, see figure 6.
D = Data pulse, see figure 6.

- 1/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or
 (b) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.
 2/ Only a summary of attributes data is required.

TABLE III. Group A inspection for device type 02
Terminal conditions (pins not designated are open)

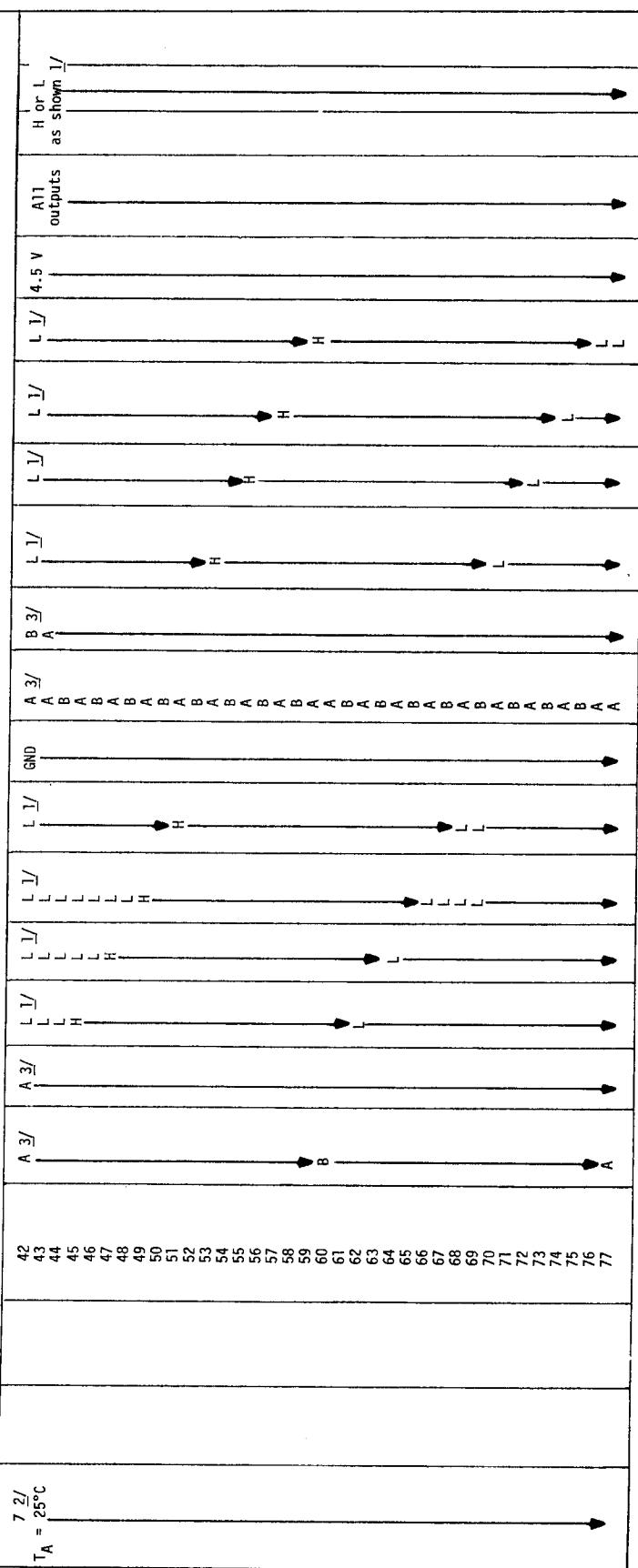
Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	Cases A, B, C, D	Input serial A	Input serial B	3	4	5	6	7	8	9	10	11	12	13	14	Test limits	
		Test No.			0 _A	0 _B	0 _C	0 _D	GND	Clock	Clear	0 _E	0 _F	0 _G	0 _H	V _{CC}	Meas: terminal	Min	Max	Unit
1	V _{OH}	3006	1	2	2.0 V	2.0 V	- .2 mA	- .2 mA	GND	C	4.5 V					4.5 V	0 _A	2.4		V
	T _A = 25°C			3													0 _B	0 _C	0 _D	0 _E
				4													0 _F	0 _G	0 _H	0 _A
				5													0 _A	0.4		
				6													0 _B	0 _C	0 _D	0 _E
				7													0 _F	0 _G	0 _H	0 _A
				8													0 _A	0.4		
				9	4.5 V	4.5 V	- .2 mA										0 _B	0 _C	0 _D	0 _E
				10	0.8 V	0.8 V	4 mA	4 mA									0 _F	0 _G	0 _H	0 _A
	V _{OL}	3007	11	12													0 _A	0.4		
			13	14													0 _B	0 _C	0 _D	0 _E
			15	16													0 _F	0 _G	0 _H	0 _A
			17	18													0 _A	0.4		
			19	20													0 _B	0 _C	0 _D	0 _E
			21	22													0 _F	0 _G	0 _H	0 _A
	I _{IL}	3009	23	24													0 _A	0.4		
			25	26													0 _B	0.35	-0.8	μA
	I _{IH1}	3010	27	28													In. ser. A	20		
			29	30													In. ser. B			
	I _{TH2}	3010	31	32													CLK			
																	CLR			

See footnotes at end of table.

TABLE III. Group A inspection for device type 02. - Continued
Terminal conditions (pins not designated are open)

tests, terminal conditions and limits as for subgroup 1, except $T_A = 125^\circ\text{C}$.

tests, terminal conditions and limits as for subgroup 1, except $T_A = -55^\circ\text{C}$.



See footnotes at end of table.

TABLE III. Group A inspection for device type 02. - Continued
Terminal conditions (pins not designated are open)

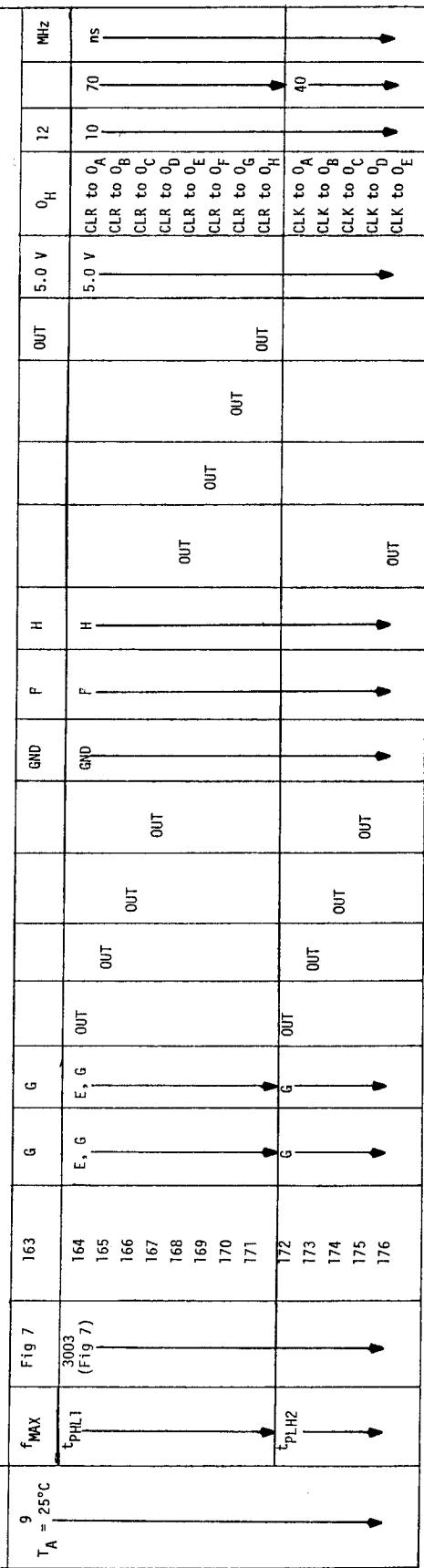
Subgroup	Symbol	MIL-STD-883 method	Cases A, B,	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test limits
			Input serial A	Input serial B	0 _A	0 _B	0 _C	0 _D	GND	Clock	Clear	0 _E	0 _F	0 _H	V _{CC}	Meas. terminal	Min. Max. Unit	
7	T _A = 25°C		78	79	A 3/V	A 3/V	L 1/V	L 1/V	GND		B	A	L 1/V	L 1/V	4.5 V	All outputs	H or L as shown 1/	
			80	81							B	A						
			82	83							B	A						
			84	85							B	A						
			86	87							B	A						
			88	89							B	A						
			90	91							B	A						
			92	93							B	A						
			94	95							B	A						
			96	97							B	A						
			98	99							B	A						
			100	101							B	A						
			102	103							B	A						
			104	105							B	A						
			106	107							B	A						
			108	109							B	A						
			110	111							B	A						
			112	113							B	A						
			114	115							B	A						
			116	117							B	A						
			118	119							B	A						
			120	121							B	A						
			122	123							B	A						
			124	125							B	A						
			126	127							B	A						
			128	129							B	A						
			130	131							B	A						
			132	133							B	A						
			134															

See footnotes at end of table.

TABLE III. Group A inspection for device type 02. - Continued
Terminal conditions (pins not designated are open)

the tests, terminal conditions and limits as for subgroup 7, except $T_a = 125^\circ\text{C}$ and -55°C .

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See footnotes at end of table.

TABLE III. Group A inspection for device type 02. - Continued

Terminal conditions (pins not designated are open)												Test limits											
Subgroup	Symbol	MTL-STD-883 method	Cases A, B, C, D	Test No.	Input serial A	Input serial B	0 _A	0 _B	0 _C	0 _D	GND	Clock	Clear	0 _E	0 _F	0 _G	0 _H	V _{CC}	Meas. terminal	Min.	Max.	Unit	
9 $T_A = 25^\circ\text{C}$	t_{PLH2}	Fig 7	177	6							GND							5.0 V	CLK to 0 _F	10	40	ns	
			178	6															CLK to 0 _G	1			
			179																CLK to 0 _H		60		
			180								OUT												
			181									OUT											
	t_{PHL2}	(Fig 7)	182									OUT											
			183										OUT										
			184											OUT									
			185												OUT								
			186													OUT							
10 $T_A = 125^\circ\text{C}$	t_{PLH1}	(Fig 7)	187																				
			188	6															OUT				
			189	E, G								OUT											
			190																				
			191																				
	t_{PLH2}	(Fig 7)	192										OUT										
			193																				
			194																				
			195																				
			196																				
11	Same tests, terminal conditions and limits as for subgroup 10, except $T_A = -55^\circ\text{C}$.																						

NOTES: C = Clock pulse, see figure 7.
D = Momentary ground then 4.5 V to clear register before start of test.
E = Outputs are set to high level prior to measurement of t_{PHL} from clear.

F = Input A from figure 7.

G = Input B from figure 7.

H = Input C from figure 7.

1/ Output voltages shall be either: (a) $H = 2.4\text{ V}$, minimum and $L = 0.4\text{ V}$, maximum when using a high speed checker double checker;
or (b) $H \geq 1.5\text{ V}$ and $L < 1.5\text{ V}$ when using a high speed checker single comparator.

2/ Only a summary of attributes data is required.
3/ Inputs: A = 2.0 Volt and B = 0.8 volt.

TABLE III. Group A inspection for device type 03
Terminal conditions (Pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits		
			Test No.	W _R	20 ₇	20 ₇	20 ₅	20 ₁	20 ₀	2CP	GND	CP COM	1CP	1B ₀	1D ₁	1D ₅	1D ₇	V _{CC}	W _R	Min	Max	Unit	
$T_4 = 25^\circ\text{C}$	I _{1L1}	3009	1	0.3 V							GND								5.5 V	W _R	-0.12	-0.4	mA
	I _{1L2}		2																10 ₀				
	I _{1L3}		3																10 ₁				
	I _{1L4}		4								0.3 V								20 ₀				
	I _{1L5}		5																20 ₁				
	I _{1L6}		6																1CP	-0.25	-0.6		
	I _{1L7}		7																2 CP	-0.25	-0.6		
	I _{1L8}		8																10 ₅	-0.24	-0.8		
	I _{1L9}		9																20 ₅	-0.24	-0.8		
	I _{1L10}		10																CP COM	-0.36	-1.2		
$T_4 = 100^\circ\text{C}$	I _{1H1}	3010	11	2.4 V							GND								W _R	20			
	I _{1H2}		12	GND															10 ₀				
	I _{1H3}		13																10 ₁				
	I _{1H4}		14																20 ₀				
	I _{1H5}		15																20 ₁				
	I _{1H6}		16																1CP	30			
	I _{1H7}		17																2CP	30			
	I _{1H8}		18																10 ₅	40			
	I _{1H9}		19																20 ₅	40			
	I _{1H10}		20																CP COM	60			
$T_4 = 150^\circ\text{C}$	I _{1S1}		21	5.5 V															W _R	100			
	I _{1S2}		22	GND															10 ₀				
	I _{1S3}		23																10 ₁				
	I _{1S4}		24																20 ₀				
	I _{1S5}		25																20 ₁				
	I _{1S6}		26																1CP				
	I _{1S7}		27																2CP				
	I _{1S8}		28																10 ₅				
	I _{1S9}		29																20 ₅				
	I _{1S10}		30																CP COM				
$T_4 = 200^\circ\text{C}$	I ₃₀₁₁		31																10 ₇	-2.5	-25	mA	
	I ₃₀₁₂		32																10 ₇	-2.5	-25	mA	

See footnote at end of table.

TABLE III. Group A inspection for device type 03. - Continued

See footnote at end of table.

TABLE III. Group A inspection for device type 03 - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		
		Test No.	NR	2Q ₇	2Q ₇	2D ₅	2D ₁	2D ₀	2CP	GND	CP COM	1CP	1D ₀	1D ₁	1D ₅	1Q ₇	1Q ₇	V _{CC}	Meas. terminal	Max. Min.	Unit	
T _A = 25°C	t _{PHL1}	3003 (Fig 8)	63	2.0 V						GND	IN							5.0 V	1CP to 1Q ₇	85 ns		
			64	2.0 V	OUT													2CP to 2Q ₇	20 ns	85		
			65	IN														NR to 1Q ₇	30 ns	110		
			66	IN	OUT	2.0 V	2.0 V	2.0 V				2.0 V	2.0 V	2.0 V	OUT			NR to 2Q ₇	30 ns	110		
	f _{MAX}		67																6 - MHz			
T _A = 125°C	t _{PHL1}	3003 (Fig 8)	68	2.0 V						IN								1CP to 1Q ₇	44 ns	55 ns		
	t _{PHL1}		69	2.0 V	OUT					IN								2CP to 2Q ₇	44 ns	55 ns		
	t _{PHL1}		70	2.0 V						IN								1CP to 1Q ₇	25 ns	100		
	t _{PHL1}		71	2.0 V	OUT					IN								2CP to 2Q ₇	25 ns	100		
	t _{PHL2}		72	IN									2.0 V	2.0 V	2.0 V	OUT			NR to 1Q ₇	32 ns	125 ns	
	t _{PHL3}		73	IN	OUT	2.0 V	2.0 V	2.0 V										NR to 2Q ₇	32 ns	125 ns		
	f _{MAX}		74																			
T _A = -55°C	t _{PHL1}		75	2.0 V						IN								1CP to 1Q ₇	44 ns	55 ns		
	t _{PHL1}		76	2.0 V	OUT					IN								2CP to 2Q ₇	44 ns	55 ns		
	t _{PHL1}		77	2.0 V						IN								1CP to 1Q ₇	25 ns	100		
	t _{PHL1}		78	2.0 V	OUT					IN								2CP to 2Q ₇	25 ns	100		

TABLE III. Group A inspection for device type Q3. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-SRD-833	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits
		Test No.	\overline{NR}	$2\overline{Q}_7$	$2\overline{Q}_7$	$2\overline{Q}_5$	$2\overline{Q}_1$	$2D_0$	$2D_P$	GND	CP	COM	$1D_P$	$1D_0$	$1D_5$	$1Q_7$	V_{CC}	Meas. terminal	Max. unit	
11	t_{PHL2}	3003 (Fig 8)	79	IN						GND		GND					5.0 V	\overline{NR} to $1Q_7$	32	125 ns
$T_A = -55^\circ C$	t_{PHL3}		80	IN	0UT	2.0 V	2.0 V			GND		GND					5.0 V	\overline{NR} to $2Q_7$	32	125 ns
	f_{MAX}			81						GND		GND					5.0 V		6	- MHz

NOTE:

A = Clock pulse (see figure 8).

TABLE III. Group A inspection for device type 04.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits
			Test No.	MRI	J	K	P ₀	P ₁	P ₂	P ₃	GND	PE	CP	Q ₁	Q ₀	V _{CC}	Q ₃	Q ₂	Q ₁	Q ₀	Max Unit
$T_A = 25^\circ C$	V_{0L}	3007	1	CP			0.7 V	0.7 V			GND	0.7 V	2.0 V				3.2 mA	4.5 V	Q_0	0.3 V	
			2																Q_1		
			3																Q_2		
			4																Q_3		
			5	2.0 V																	
	V_{0H}	3006	6																		
			7																		
			8																		
			9																		
			10																		
	I_{TH1}	3010	11	2.4 V																	
			12																		
			13																		
			14																		
			15																		
			16																		
			17																		
	I_{TH2}		18																		
	I_{TH3}		19																		
	I_{TH4}		20	5.5 V																	
			21	5.5 V																	
			22																		
			23																		
			24																		
			25																		
			26																		
			27																		
			28																		
	I_{OS}	3011	29	4.5 V																	
			30																		
			31																		
			32																		
			33																		
	I_{TL1}	3009	34	GND	0.3 V	4.5 V	0.3 V														
			35	CP	4.5 V	0.3 V															
			36	0.3 V																	

See footnotes at end of table.

TABLE III. Group A inspection for device type 04. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL- STD-383 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits		
			Test No.	NR	J	K	P ₀	P ₁	P ₂	P ₃	GND	PE	CP	Q ₃	Q ₀	Q ₁	Q ₂	V _{CC}	Meas. terminal	Min	Max	Unit
T _A = 25°C	I _{IL1}	3009	37				0.3 V		0.3 V		GND							5.5 V	P ₀	-1.2	-0.4	mA
	I _{IL2}		38															P ₁				
	I _{IL3}		39															P ₂				
	I _{IL3}		40															P ₃				
	I _{IL2}		41																			
	I _{IL3}		42																			
	V _{IC}		43				-10 mA															
	V _{IC}		44					-10 mA														
	V _{IC}		45						-10 mA													
	V _{IC}		46							-10 mA												
	V _{IC}		47								-10 mA											
	V _{IC}		48									-10 mA										
	V _{CC}		49										-10 mA									
	V _{CC}		50				CP															
	V _{CC}		3005																			
2	Same tests, terminal conditions and limits as for subgroup 1, except T _A = 125°C and VIC tests are omitted.																					
3	Same tests, terminal conditions and limits as for subgroup 1, except T _A = -55°C and VIC tests are omitted.																					
7	T _A = 25°C	Truth table tests	51	B	B	B	B	B	B	B	5.5 V	5.5 V	5.5 V	GND	5.5 V	A	B	A	B	A	B	
			52	A																		
			53																			
			54																			
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			78																			

See
note 1

TABLE III. Group A inspection for device type 06. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Test limits
			Test No.	NR	J	K	P ₀	P ₁	P ₂	P ₃	GND	PE	CP	Q̄ ₃	Q ₃	Q ₂	Q ₁	Q ₀	V _{CC}	Meas. terminal
7	Truth table tests	T _A = 25°C	79	B	A															5.5 V
			80	A																L
			81	B																H
			82	B																L
			83	B																H
			84	B																L
			85	B																H
			86	B																L
			87	B																H
			88	B																L
			89	B																H
			90	B																L
			91	B																H
			92	B																L
			93	B																H
			94	B																L
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			97	B																H
			98	B																L
			99	B																H
			100	B																L
			101	B																H
			102	B																L
			103	B																H
			104	B																L
			105	B																H
			106	B																L
			107	B																H
			108	B																L
			109	B																H
			110	B																L
			111	B																H
			112	B																L
			113	B																H
			114	B																L
			115	B																H
			116	B																L
			117	B																H
			118	B																L
			119	B																H
			120	B																L
			121	B																H
			122	B																L
			123	B																H
			124	B																L
			125	B																H
			126	B																L
			127	B																H
			128	B																L
			129	B																H
			130	B																L
			131	B																H
			132	B																L
			133	B																H
			134	B																L
			135	B																H

See note 1

See footnotes at end of table.

TABLE III. Group A inspections for device type 04. - Continued

Subgroup	Symbol	MIL-STD-883 method	Terminal conditions (pins not designated are open)																Meas. terminal	Test limits
			Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
7	Truth table tests		136	A	GND	5.5 V														
			137	A																
			138																	
			139																	
			140																	
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See note 1

See footnotes at end of table.

TABLE III. Group A inspection for device type 04. - Continued
Terminal conditions (pins not designated are open)

See footnotes at end of table.

TABLE III. Group A inspection for device type 04. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL- STD-883 method	Cases E, F		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Meas. terminal	Test limits
			Test No.	MR	J	K	P ₀	P ₁	P ₂	P ₃	GND	PE	CP	Q ₃	Q ₂	Q ₁	Q ₀	V _{CC}	Min	Max	Unit	
10 $T_A = 125^\circ C$	t_{PHL1}	3003 (Fig. 9)	233	2.4 V	2.4 V	GND	2.4 V	2.4 V	2.4 V	2.4 V	GND	2.4 V	IN	OUT	OUT	OUT	OUT	5.0 V	Q ₃	25	100	ns
	t_{PHL2}		234																Q ₂			
	t_{PHL3}		235																Q ₁			
	f_{SR}	Fig. 9	237	IN															Q ₀	30	100	
	t_{PHL1}		238																Q ₁			
	t_{PHL2}		239															Q ₂				
11 $T_A = -55^\circ C$	t_{PHL1}	240																	Q ₃			
	t_{PHL3}		241																Q ₃	35	120	Hz
	f_{SR}	Fig. 9	242	2.4 V															OUT			
	t_{PHL1}		243																IN			
	t_{PHL2}		244																OUT			
	t_{PHL3}		245																Q ₀	14	65	ns
	t_{PHL1}		246																Q ₁			
	t_{PHL2}		247																Q ₂			
	t_{PHL3}		248																Q ₃			
	f_{SR}	Fig. 9	249																IN			
	t_{PHL1}		250																OUT			
	t_{PHL2}		251																OUT			
	t_{PHL1}		252																OUT			
	t_{PHL2}		253	IN															OUT			
	t_{PHL3}		254																OUT			
	f_{SR}	Fig. 9	255																OUT			
	t_{PHL1}		256																OUT			
	t_{PHL2}		257																OUT			
	t_{PHL1}		258	2.4 V															IN			
	t_{PHL2}																		IN			
	t_{PHL3}																		IN			
	f_{SR}																		IN			
	t_{PHL1}																		IN			
	t_{PHL2}																		IN			

NOTES:

1. INPUTS: A = 2.0 Volts and B = GND
OUTPUTS: Output voltage shall be either
(a) H = 2.4 volts minimum and L = 0.4 volt maximum when using a high-speed checker double comparator or
(b) H ≥ 1.5 volts and L < 1.5 volts when using a high-speed checker single comparator.
2. The term P-XX means that the affected pin is connected to pin XX for the test.
3. See figure 9 for CP.

TABLE III. Group A inspection for device type 05.
Terminal conditions (pins not designated are open)

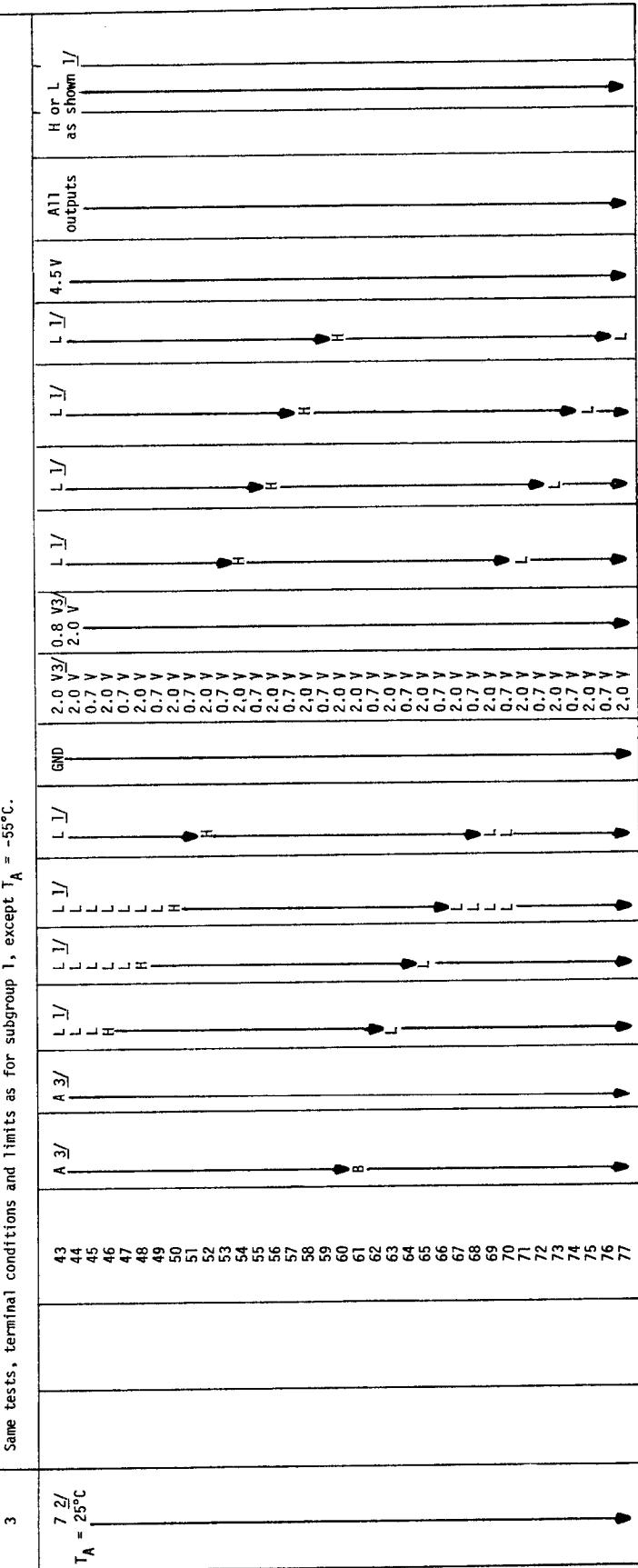
Subgroup	Symbol	MIL-STD-883 Test No.	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Test limits	
				Input serial A	Input serial B	0_A	0_B	0_C	0_D	GND	Clock	Clear	0_E	0_F	0_G	0_H	V_{CC}	Min	Max	Unit
1 $T_A = 25^\circ C$	V_{OH}	3006		2.0 V	2.0 V	-2 mA	-2 mA	-2 mA	-2 mA	GND	C	4.5 V					4.5 V	0.4 A	2.4	V
	V_{OL}	3007		0.7 V	0.7 V	2 mA	2 mA	2 mA	2 mA	4.5 V							0.3 V			
	I_{IH1}	3009		0.3 V	4.5 V												In. ser. A	-0.06 - 18	mA	
	I_{IH2}	3010		2.4 V	GND												In. ser. B	-0.12 - 36	mA	
	I_{IH3}			2.4 V	GND												CLK	10	μA	
	I_{IH4}			5.5 V	GND												CLR	20	μA	
				5.5 V	GND												In. ser. A	100	μA	
																	CLR	200	μA	

See footnotes at end of table.

TABLE III. Group A inspection for device type 05. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Test Limits			
			Cases A, B, C, D	Test No.	Input serial A	Input serial B	0_A	0_B	0_C	0_D	GND	Clock	Clear	0_E	0_F	0_G	0_H	V _{CC}	Meas. terminal	Min	Max
1	I _{GS}	3011			33	4.5 V	4.5 V	GND			GND		A	4.5 V			5.5 V	0 A	-3	-15	mA
			T _A = 25°C		34													0 B	0 C	0 D	
					35													0 E	0 F	0 G	
					36													0 H			
					37																
					38																
					39																
					40																
	I _{CC1}	3005			41												0.3 V	D			
	I _{CC2}	3005			42												2.4 V	D			
																	V _{CC}	V _{CC}	V _{CC}		
																		9	9	9	

Same tests, terminal conditions and limits as for subgroup 1, except $T_A = 125^\circ\text{C}$.



See footnotes at end of table.

TABLE III. Group A inspection for device type 05 - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	All outputs	Test limits																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																										
					A	A	A	A	A	0 _D	0 _E	0 _F	0 _G	0 _H	V _{CC}					H or L as shown 1/																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																											
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373	80374	80375	80376	80377	80378	80379	80380	80381	80382	80383	80384	80385	80386	80387	80388	80389	80390	80391	80392	80393	80394	80395	80396	80397	80398	80399	80400	80401	80402	80403	80404	80405	80406	80407	80408	80409	80410	80411	80412	80413	80414	80415	80416	80417	80418	80419	80420	80421	80422	80423	80424	80425	80426	80427	80428	80429	80430	80431	80432	80433	80434	80435	80436	80437	80438	80439	80440	80441	80442	80443	80444	80445	80446	80447	80448	80449	80450	80451	80452	80453	80454	80455	80456	80457	80458	80459	80460	80461	80462	80463	80464	80465	80466	80467	80468	80469	80470	80471	80472	8

TABLE III. Group A inspection for device type 05. - Continued
Terminal conditions (pins not designated are open)

See footnotes at end of table.

TABLE III. Group A inspection for device type 05. - Continued
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Cases A, B, C, D	Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	V_{CC}	Meas. terminal	Test limits
9 $T_A = 25^\circ\text{C}$	t_{PHL2}	3003 (Fig 10)	181 182 183 184 185 186 187 188	G OUT OUT OUT OUT OUT OUT OUT	G OUT OUT OUT OUT OUT OUT OUT	GND GND GND GND GND GND GND GND	F H F H F H F H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	5.0 V 5.0 V 5.0 V 5.0 V 5.0 V 5.0 V 5.0 V 5.0 V	CLK to O _A CLK to O _B CLK to O _C CLK to O _D CLK to O _E CLK to O _F CLK to O _G CLK to O _H	120 ns 120 ns 120 ns 120 ns 120 ns 120 ns 120 ns 120 ns	Unit								
10 $T_A = 125^\circ\text{C}$	f_{MAX}	(Fig 10)	189 190 191 192 193 194 195 196 197	G E, G OUT OUT OUT OUT OUT OUT OUT	G E, G OUT OUT OUT OUT OUT OUT OUT	GND GND GND GND GND GND GND GND GND	F H F H F H F H F	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	3 Hz 3 Hz 3 Hz 3 Hz 3 Hz 3 Hz 3 Hz 3 Hz	Hz								
	t_{PHL1}	3003 (Fig 10)	190 191 192 193 194 195 196 197	G E, G OUT OUT OUT OUT OUT OUT	G E, G OUT OUT OUT OUT OUT OUT	GND GND GND GND GND GND GND GND	F H F H F H F H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	140 ns 140 ns 140 ns 140 ns 140 ns 140 ns 140 ns 140 ns	ns								
	t_{PLH2}		198 199 200 201 202 203 204 205	G OUT OUT OUT OUT OUT OUT OUT	G OUT OUT OUT OUT OUT OUT OUT OUT	GND GND GND GND GND GND GND GND	F H F H F H F H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	120 ns 120 ns 120 ns 120 ns 120 ns 120 ns 120 ns 120 ns	ns								
	t_{PLH2}		206 207 208 209 210 211 212 213	OUT OUT OUT OUT OUT OUT OUT OUT	OUT OUT OUT OUT OUT OUT OUT OUT	GND GND GND GND GND GND GND GND	F H F H F H F H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	0 _A 0 _B 0 _C 0 _D 0 _E 0 _F 0 _G 0 _H	120 ns 120 ns 120 ns 120 ns 120 ns 120 ns 120 ns 120 ns	ns								

11 Same tests, terminal conditions and limits as for subgroup 10, except $T_A = -55^\circ\text{C}$.

NOTES: C = Clock pulse (see figure 7).

D = Momentary ground then 4.5 V to clear register before start of test.

E = Outputs are set to high level prior to measurement of t_{PHL} from clear.

F = Input A from figure 7.

G = Input B from figure 7.

H = Input C from figure 7.

1/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.

2/ Only a summary of attributes data is required.

INPUTS: A = 2.0 Volts and $\beta = 0.7$ Volt.

- (c) Requirement for certificate of compliance, if applicable.
- (d) Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.
- (e) Requirements for packaging and packing.
- (f) Requirements for failure analysis (including required test condition of method 5003), corrective action and reporting of results, if applicable.
- (g) Requirements for product assurance options.
- (h) Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313, MIL-STD-1331, and as follows:

GND	- - - - -	Electrical ground (common terminal)
V _{IN}	- - - - -	Voltage level at an input terminal
I _{IN}	- - - - -	Current-flowing into an input terminal

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer lead lengths and lead forming shall not affect the part number.

6.6 Substitutability. Microcircuits covered by this specification are substitutable for the following commercial device types:

<u>Device type</u>	<u>Commercial type</u>
01	54L95
02	54L164
03	93L28
04	93L00
05	76L70

Custodian:
Air Force - 17

Preparing activity:
Air Force - 17

Review activities:
Air Force - 11, 17, 80, 85
DSA - ES

Agent:
DSA - ES
(Project 5962-F056)

User activity:
Air Force - 19